ATRIA INSTITUTE OF TECHNOLOGY

ATRIA INSTITUTE OF TECHNOLOGY 1st Main, AG's Colony, Anandanagar, Bangalore- 560024
Department of Electronics and Communication

ELECTRONINC DEVICES AND INSTRUMENTATION LAB
SUB: 18ECL37 **CLASS : III A,B,C**

ELECTRONIC DEVICES AND INSTRUMENTATION LABORATORY SEMESTER – III (EC/TC) [As per Choice Based Credit System (CBCS) scheme]			
Laboratory Code	**18ECL37**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02 Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**
CREDITS – 02			

Course objectives: This laboratory course enables students to

- Understand the circuit schematic and its working
- Study the characteristics of different electronic devices
- Design and test simple electronic circuits as per the specifications using discrete electronic components.
- Familiarize with EDA software which can be used for electronic circuit simulation.

Laboratory Experiments

PART A : Experiments using Discrete components

1. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative)
2. Half wave rectifier and Full wave rectifier with and without filter and measure the ripple factor
3. Characteristics of Zener diode and design a Simple Zener voltage regulator determine line and load regulation
4. Characteristics of LDR and Photo diode and turn on an LED using LDR
5. Static characteristics of SCR.
6. SCR Controlled HWR and FWR using RC triggering circuit
7. Conduct an experiment to measure temperature in terms of current/voltage using a temperature sensor bridge.
8. Measurement of Resistance using Wheatstone and Kelvin's bridge.

PART-B : Simulation using EDA software (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any equivalent tool)

1. Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
2. Transfer and drain characteristics of a JFET and MOSFET.
3. UJT triggering circuit for Controller Rectifiers.

4. Design and simulation of Regulated power supply.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Understand the characteristics of various electronic devices and measurement of parameters.
- Design and test simple electronic circuits
- Use of circuit simulation software for the implementation and characterization of electronic circuits and devices.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-A** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

CONTENTS:

1.Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative)

Aim:

Design and obtain the transfer characteristics of different peak clipping circuits.

1. Positive peak clipping (shunt and series)
2. Negative peak clipping (shunt and series)
3. Double ended clipping
4. Slicer

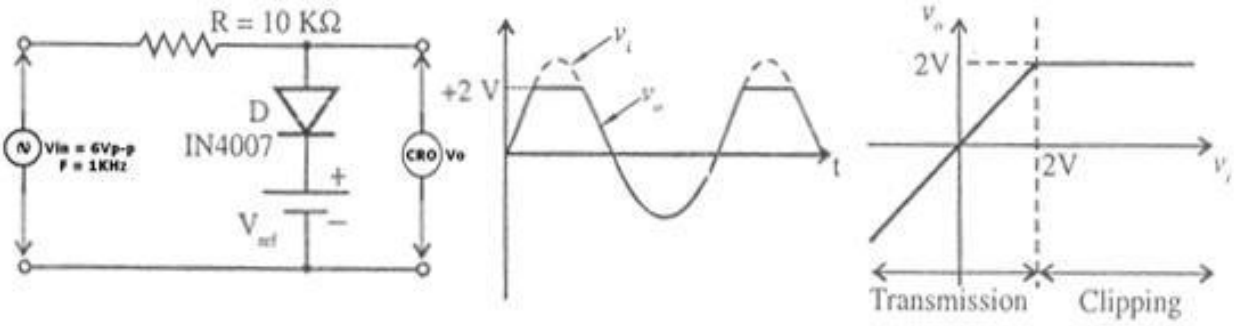
Components:

Sl no.	Components required	Range	Qty
1.	Diodes	1N 4007	2
2.	Resistors	10KΩ	1
3.	CRO		1
4.	Power supply (VRPS)	0-30 V	2
5.	Signal Generator		1
6.	Capacitor	1uF	1
			1

I) Peak clipping circuits

a) Diode shunt clipping above V_{Ref} (reference voltage) / Positive peak clipping

Circuit Diagram:



Design : Let the output be clipped to say +2V. $\therefore V_o(max) = +2V$

from circuit diagram,

$$\mathbf{V_o(max) = V_D + V_{REF}}$$

Where V_D is the diode drop $\cong$ 0.7V

$\therefore V_{REF} = V_o(max) - V_D$

$= 2.0 - 0.7 = 1.3V$

Choose $\mathbf{R = \sqrt{(R_f * R_r)}}$

$= 10K\Omega$,

where R_f (diode forward resistance) =10Ω.

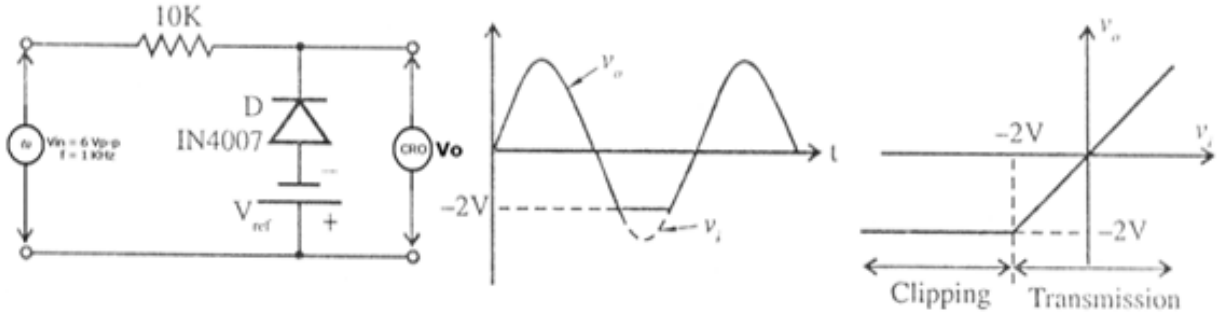
Choose R_r (diode reverse resistance) = 10MΩ

Procedure:

- Connections are made as shown in the circuit diagram.
- The input sinusoidal Signal (V_i) is set to 6V (p-p) of 1KHz frequency.
- Observe the output Waveform (V_O) on the CRO and verify it with the expected waveforms.
- To find the transfer characteristics of the waveforms, apply V_i and V_o to the X and Y channel of the CRO and Use XY mode for observation.

b) Diode shunt clipping below V_{Ref} (reference voltage) / Negative peak clipping

Circuit Diagram:



Design:

Let the output be clipped at -2V. $\therefore V_O = -2V$

from circuit diagram,

$\mathbf{V_O = -V_D + V_{REF}}$

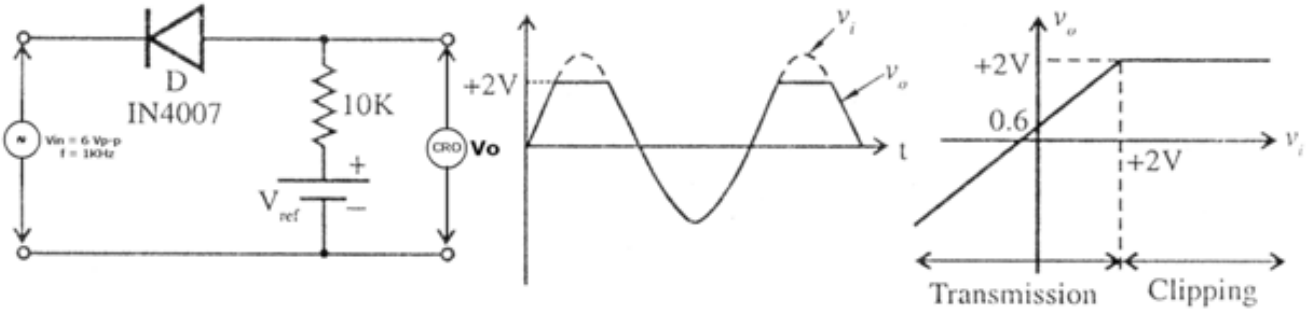
Where V_D is the diode drop $\cong$ 0.7V

$\therefore V_{REF} = V_O + V_D$

$= - 2.0 + 0.7 = - 1.3$ V

c) Diode series clipping above V_{Ref} (reference voltage) / Positive peak clipping

Circuit Diagram:



Design:

Let the output be clipped at +2V.

$\therefore$ **$V_O = V_{REF}$**

= +2V

Choose **$R = \sqrt{(R_f * R_r)}$** = 10KΩ,

where R_f is the diode forward resistance = 10Ω.

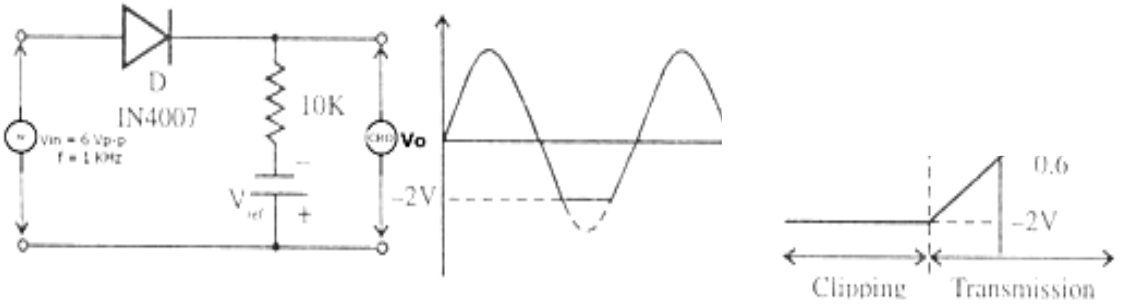
Choose R_r (reverse resistance of the diode) = 10MΩ

Procedure:

- Connections are made as shown in the circuit diagram.
- The input sinusoidal Signal (V_i) from the signal generator is set to 6V (p-p) of 1KHz frequency.
  Observe the output Waveform (V_o) on the CRO and verify it with the expected waveforms.
- To find the transfer characteristics of the waveforms, apply V_i and V_o to the X and Y channel of the CRO. Use XY mode for observation.

d) Diode series clipping below V_{Ref} (reference voltage) / Negative peak clipping

Circuit Diagram :



Design:

Let the output be clipped at -2V.

$\therefore$ **$V_O = V_{REF}$** = -2V

Choose **$R = \sqrt{(R_f * R_r)}$** = 10KΩ,

where R_f is the diode forward resistance = 10Ω.

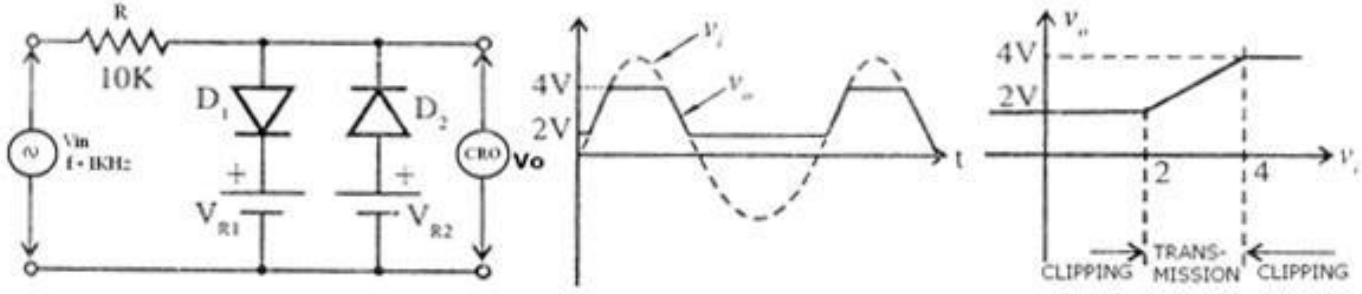
Choose R_r (reverse resistance of the diode) = 10MΩ

Procedure :

- Connections are made as shown in the circuit diagram.
- The input sinusoidal Signal (V_i) from the signal generator is set to 6V(p-p) of 1KHz frequency.
- Observe the output Waveform(V_o) on the CRO and verify it with the expected waveforms.
- To find the transfer characteristics of the waveforms, apply V_i and V_o to the X and Y channel of the CRO. Use X-Y mode for observation.

e) Clipping at two independent levels (Slicer)

Circuit Diagram:



Design :

To obtain a slice of input voltage betwee

Let $V_{REF1} > V_{REF2}$.

To find V_{REF1}:

$V_o = V_{REF1} + V_D$

Where V_D is the diode drop $\cong$ 0.7V

Since V_o = 4V,

$\therefore V_{REF1} = V_o - V_D$

= 4.0 – 0.7

= 3.3 V

To find V_{REF2}:

$V_o = V_{REF2} - V_D$

Where V_D is the diode drop ≅ 0.7V

Since V_o = 2V,

$\therefore V_{REF2} = V_o + V_D$

= 2.0 + 0.7

=2.7 V

Choose **R = sqrt(R_f * R_r)** = 10KΩ,

where R_f is the diode forward resistance = 10Ω.

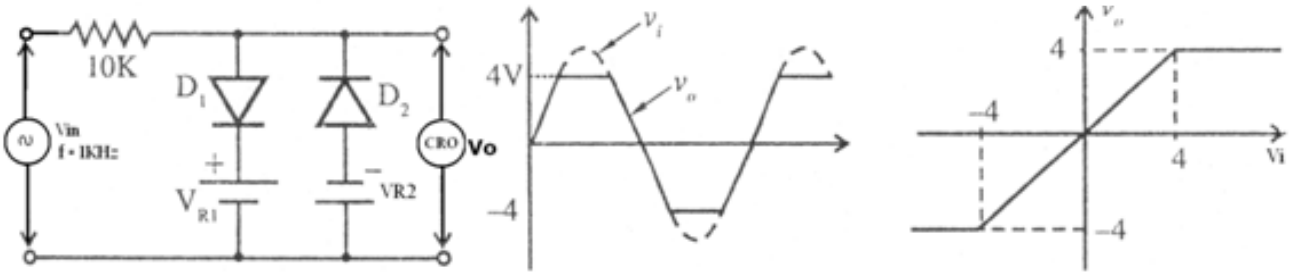
Choose R_r (reverse resistance of the diode) = 10MΩ

Procedure:

- Connections are made as shown in the circuit diagram.
- The input sinusoidal Signal (V_i) is set to 10V(p-p) of 1KHz frequency.
- Observe the output Waveform (V_o) on the CRO and verify it with the expected waveforms.
- To find the transfer characteristics of the waveforms, apply V_i and V_o to the X and Y channel of the CRO. Use X-Y mode for observation.

**B) Double Ended Clipper with symmetrical **

Circuit Diagram:



Design:

Let the output be clipped at +4V and -4V.

$\therefore$ Vo(max) = +4 V and Vo(min) = -4 V

To find V_{REF1}:

V_o (max) = V_{REF1} + V_D

Where V_D is the diode drop ≅ 0.7 V

$\therefore V_{REF1}$ = Vo(max) –V_D

= 3.3 V

To find V_{REF2}:

V_o (min) = V_{REF2} - V_D

Where V_D is the diode drop ≅ 0.7 V

$\therefore V_{REF2} = Vo(min) + V_D$

$= - 3.3$ V

Choose **R = √(R_f * R_r)** = 10KΩ,

Where R_f is the diode forward resistance = 10Ω.

Choose R_r (reverse resistance of the diode) = 10MΩ

Procedure:

- Connections are made as shown in the circuit diagram.
- The input sinusoidal Signal (V_i) from the signal generator is set to 10V(p-p) of 1KHz frequency.
- Observe the output Waveform (V_o) on the CRO and verify it with the expected waveforms.
- To find the transfer characteristics of the waveforms, apply V_i and V_o to the X and Y channel of the CRO. Use X-Y mode for observation.

Diode Clamping Circuits

Aim :

Design and testing of clamping circuits

a) Positive peak clamping

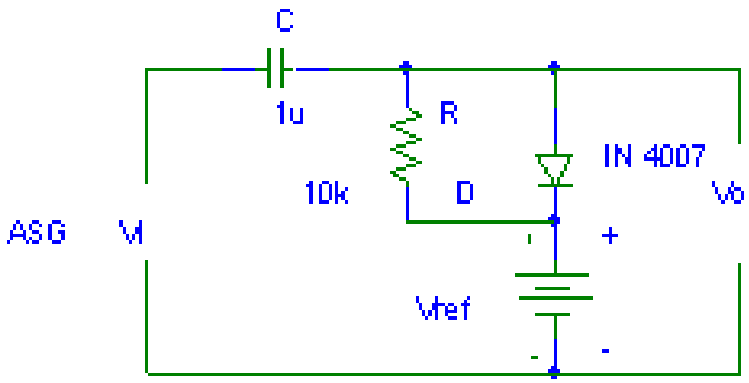
b) negative peak clamping.

Components :

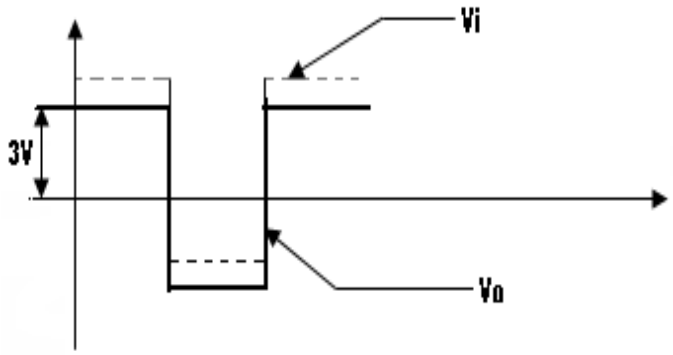
Sl no.	Components required	Range	Qty
1.	Diodes	1N 4007	1
2.	Resistors	10KΩ	1
3.	Capacitor	1µF	1
4.	CRO		1
5.	Power supply (VRPS)	0-30 V	1
6.	Signal Generator		1

a) Positive Peak Clamper (Negative clamper)

Circuit Diagram:



Expected waveform:



Design :

To design a clamping circuit to clamp the positive peak at 3V. The input waveform has a frequency of 1KHz sine wave or square wave.

V_O = +3V

Design of V_{REF} :

From circuit diagram,

$$\mathbf{V_O = V_D + V_{REF}}$$

Where V_D is the diode drop $\cong$ 0.7V

$$\therefore V_{REF} = Vo - V_D$$

$$= 3.0 - 0.7$$

$$= 2.3 \text{ V}$$

Design of C:

For a given frequency of 1KHz, T=1msec

Choose RC >> T (so that tilt in the waveform is negligible)

Let RC = 10T

ie. RC = 10 * 1msec

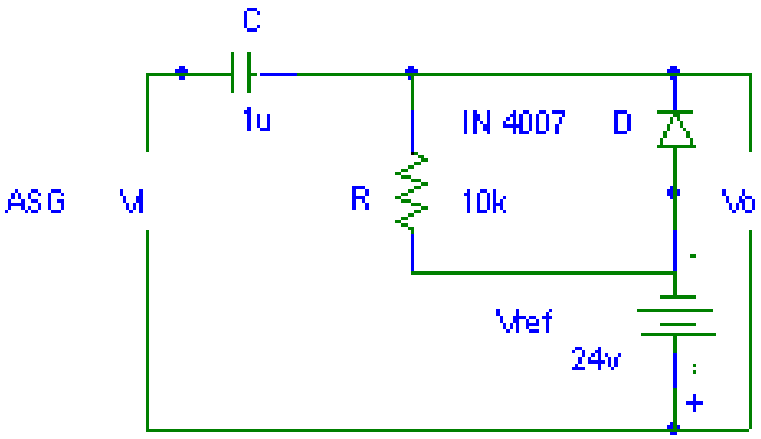
$\therefore C = 10ms / 10K\Omega$

$= 1\mu F$

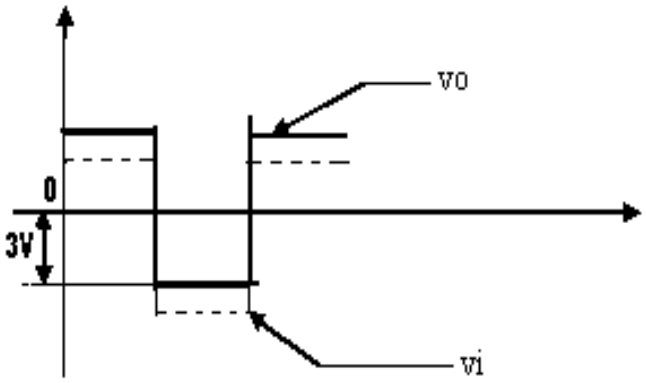
Procedure:

- Connections are made as shown in the circuit diagram.
- The input square Signal (V_i) from the signal generator is set to 8V(p-p) of 1KHz frequency (peak amplitude of input must be greater than the clamping level).
- Observe the output Waveform (V_O) on the CRO and verify it with the expected waveforms.

b) Negative Peak Clamper (positive clamper)
Circuit Diagram:



Expected waveform:



Design:

To design a clamping circuit to clamp the negative peak at -3V.

Design of V_{REF} :

V_O = -3V

From circuit diagram,

$V_O = V_{REF} – V_D$

Where V_D is the diode drop $\cong$ 0.7V

$\therefore V_{REF} = Vo + V_D$

= -3.0 + 0.7

= -2.3 V

Design of C:

For a given frequency of 1KHz, T=1msec

Choose RC >> T (so that tilt in the waveform is negligible)

Let RC = 10T

ie. RC = 10 * 1msec

$\therefore$C = 10ms / 10KΩ = 1μF

Procedure:

- Connections are made as shown in the circuit diagram.
- The input square Signal (V_i) from the signal generator is set to 8V(p-p) of 1KHz frequency (peak amplitude of input must be greater than the clamping level).
- Observe that the negative peak of the output Waveform (V_O) is clamped to 0V on the CRO when V_{REF} = 0 and verify it with the expected waveforms.

Result:

RESULT:

Thus the operation of clipper and clamper circuits have been observed and verified

2. Half wave rectifier and Full wave rectifier with and without filter and measure the ripple factor

AIM:

To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full-wave rectifier center tapped circuit with and without Capacitor filter.

APPARATUS:

S. No.	Name	Range/Value	Quantity
1	Transformer	230V / 9-0-9V	1
2	Diode	1N4001	2
3	Capacitors	1000□F/16 V, 470□f/25V	1
4	Decade Resistance Box	-	1
5	Multimeter	-	1
6	Bread Board and connecting wires	-	1
7	Dual Trace CRO	20MHz	1

PROCEDURE:

Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$

Calculate Percentage of Regulation, $\%\eta = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{no load}}} * 100\%$

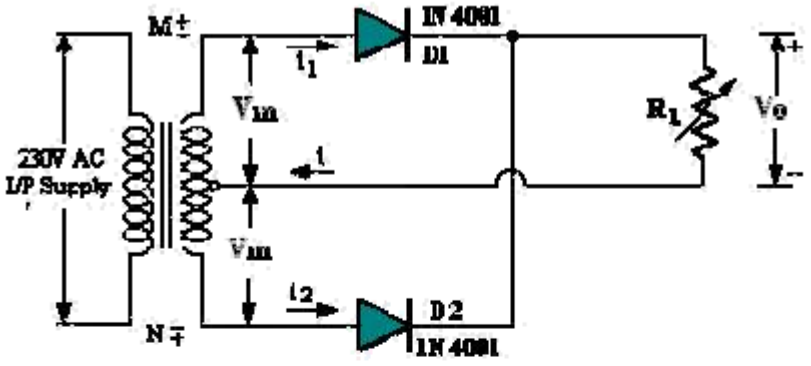
WITHOUT FILTER:

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the R_L value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 1KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance (DRB) and note down no load voltage Vdc ($V_{\text{no load}}$)
6. Connect load resistance at 1KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.

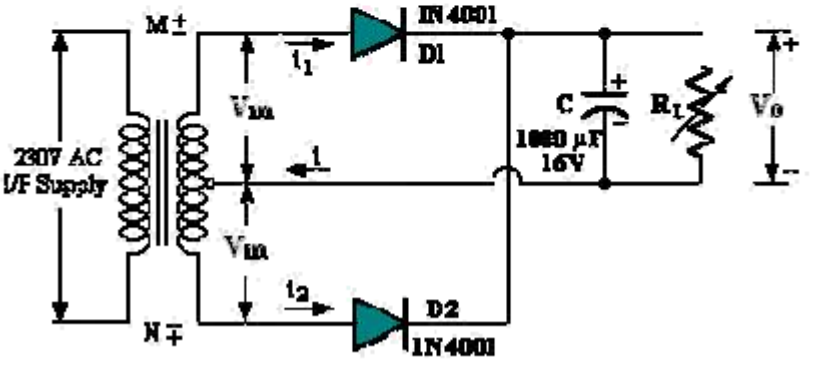
WITH CAPACITIVE FILTER:

1. Connecting the circuit as per the circuit diagram and repeat the same from steps 2 to 8.

CIRCUIT DIAGRAMS:
WITHOUT FILTER AND WITH FILTER:

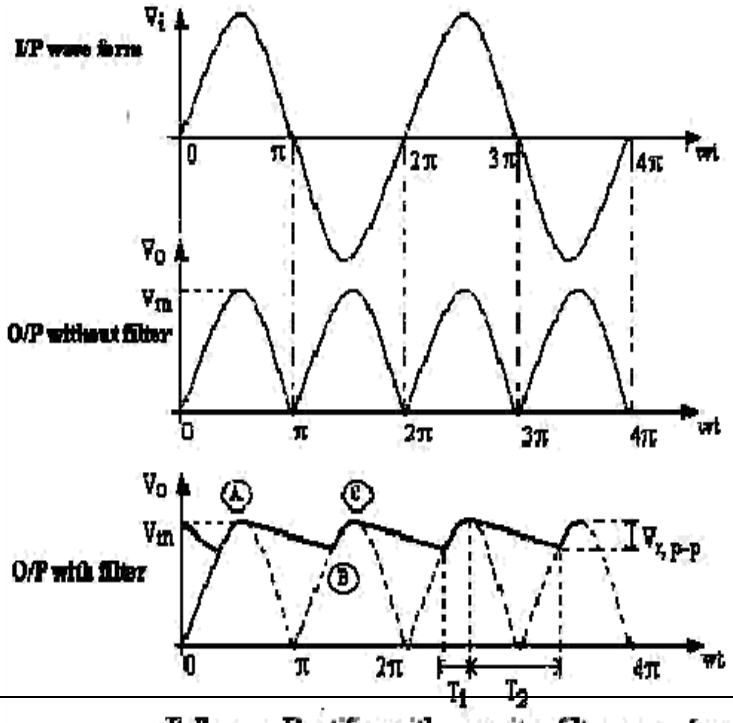


Full-wave Rectifier without filter



Full wave Rectifier with capacitor filter

WAVE SHAPES:



Full-wave Rectifier with capacitor filter wave form

WITHOUT FILTER:

V no load Voltage (Vdc) = V

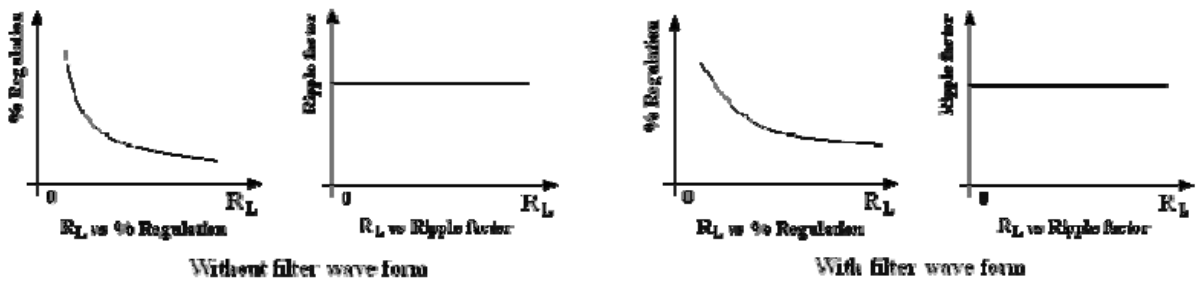
S.No	Load Resistance R_L (Ω)	O/P Voltage (Vo) V_{ac} (V)	V_{dc} (V)	Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%\right)$
1	100				
2	200				
3	300				
4	400				
5	500				
6	600				
7	700				
8	800				
9	900				
10	1K				

WITH CAPACITOR FILTER:

V no load Voltage (Vdc) = V

S.No	Load Resistance R_L (Ω)	O/P Voltage (Vo) V_{ac} (V)	V_{dc} (V)	Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%\right)$
1	100				
2	200				
3	300				
4	400				
5	500				
6	600				
7	700				
8	800				
9	900				
10	1K				

MODEL GRAPHS:



Without filter wave form

With filter wave form

RESULT: Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full-wave rectifier with and without filter.

Without Filter:

Ripple Factor : Regulation :

With Capacitor Filter:

Ripple Factor : Regulation

Half-wave rectifier

In a half-wave rectifier circuit (Fig. 1), during the positive half-cycle of the input, the diode is forward biased and conducts. Current flows through the load and a voltage is developed across it. During the negative half-cycle, it is reverse bias and does not conduct. Therefore, in the negative half cycle of the supply, no current flows in the load resistor as no voltage appears across it. Thus the dc voltage across the load is sinusoidal for the first half cycle only and a pure a.c. input signal is converted into a unidirectional pulsating output signal.

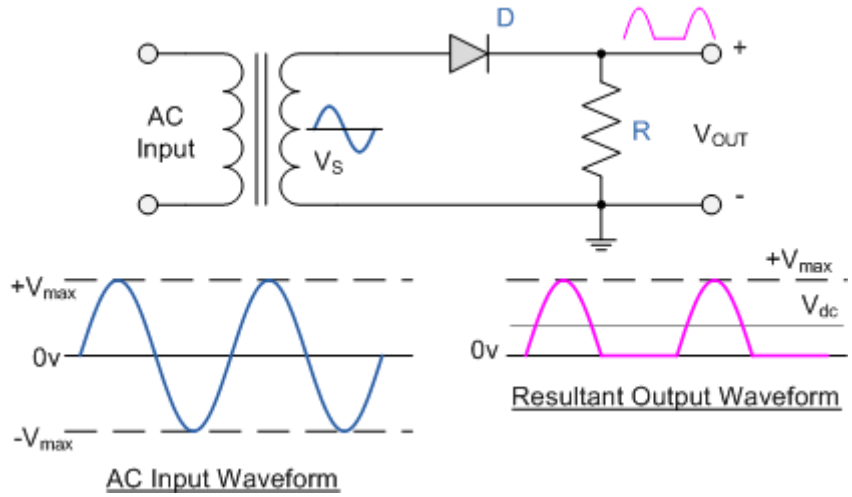


Fig.1: Half-wave rectifier circuit

Since the diode conducts only in one half-cycle (0-π), it can be verified that the d.c. component in the output is V_{max}/π, where V_{max} is the peak value of the voltage.

Ripple factor:

As the voltage across the load resistor is only present during the positive half of the cycle, the resultant voltage is "ON" and "OFF" during every cycle resulting in a low average dc value. This variation on the rectified waveform is called "**Ripple**" and is an undesirable feature. The ripple factor is a measure of purity of the d.c. output of a rectifier and is defined as

$$r = \frac{V_{dc}(output)}{V_{dc}(output)} = \sqrt{\frac{V_{rms}^2 - V_{dc}^2}{V_{dc}^2}} = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1} = \sqrt{\left(\frac{0.5}{0.318}\right)^2 - 1} = 1.21$$

In case of a half-wave rectifier $V_{rms} = V_{max}/2 = 0.5V_{max}$. (How?)

Rectification Efficiency:

Rectification efficiency, η, is a measure of the percentage of total a.c. power input converted to useful d.c. power output.

$$\eta = d.c.\,power\ delivered\ to\ load\ /\ a.c.\,power\ at\ input$$

$$= \frac{V_{dc}^{\ 2}/R_L}{V_s^{\ 2}/(r_d + R_L)} = \frac{(0.318V_{\max})^2}{(0.5V_{\max})^2\left(1 + \frac{r_d}{R_L}\right)} = \frac{0.405}{\left(1 + \frac{r_d}{R_L}\right)}$$

Here r_d is the forward resistance of diode. Under the assumption of no diode loss (r_d<<), the rectification efficiency in case of a half-wave rectifier is approximately 40.5%.

Filters:

The output of a rectifier gives a pulsating d.c. signal (Fig.1) because of presence of some a.c. components whose frequency is equal to that of the a.c. supply frequency. Very often when rectifying an alternating voltage we wish to produce a "steady" direct voltage free from any voltage variations or ripple. Filter circuits are used to smoothen the output. Various filter circuits are available such as shunt capacitor, series inductor, choke input LC filter and π-filter etc. Here we will use a simple **shunt capacitor** filter circuit (Fig. 2). Since a capacitor is open to d.c. and offers low impedance path to a.c.

current, putting a capacitor across the output will make the d.c. component to pass through the load resulting in small ripple voltage.

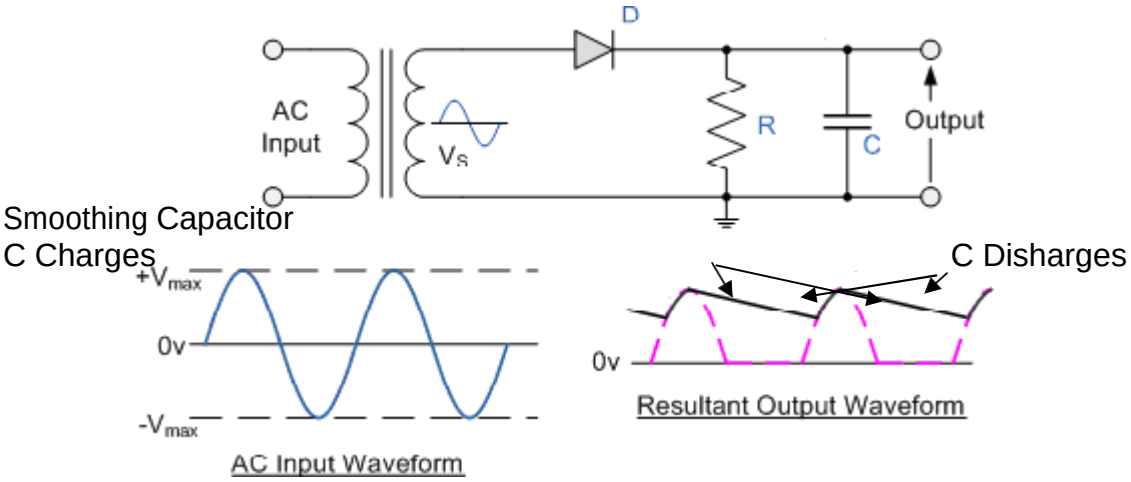


Fig.2: Half-wave rectifier circuit with capacitor filter

The working of the capacitor can be understood in the following manner. When the rectifier output voltage is increasing, the capacitor charges to the peak voltage V_m. Just past the positive peak the rectifier output voltage tries to fall. As the source voltage decreases below V_m , the capacitor will try to send the current back to diode making it reverse biased. Thus the diode separates/disconnects the source from the load and hence the capacitor will discharge through the load until the source voltage becomes more than the capacitor voltage. The diode again starts conducting and the capacitor is again charged to the peak value V_m and the process continues. Although in the output waveform the discharging of capacitor is shown as a straight line for simplicity, the decay is actually the normal exponential decay of any capacitor discharging through a load resistor. The extent to which the capacitor voltage drops depends on the capacitance and the amount of current drawn by the load; these two factors effectively form the RC time constant for voltage decay. A proper combination of large capacitance and small load resistance can give out a steady output.

Circuit components:

(ii) A step-down transformer, (ii) A junction diode, (iii) 3 Load resistors, (iv) Capacitor,

(v) Oscilloscope, (vi) Multimeter, (vii) Connecting wires, (viii) Breadboard.

Circuit Diagram: (As shown in Fig. 1 and 2)

Procedure:

i) Configure the half-wave rectifier circuit as shown in the circuit diagram. Note down all the values of the components being used.

ii) Connect the primary side of the transformer to the a.c. Mains and secondary to the input of the circuit.

iii) Feed the input and output to the two channels of oscilloscope (we will use oscilloscope here only to trace the output waveform) and save the data for each measurement.

iv) Measure the input a.c. voltage and the output a.c. and d.c. voltages using multimeter for at least 3 values of load resistor (Be careful to choose proper settings of multimeter for ac and dc measurement).

v) Multiply the V_{ac} at the input by $\sqrt{2}$**?** to get the peak value and calculate V_{dc} Using the formula $V_{dc} = V_{max}/ \pi$. Compare this value with the measured V_{dc} at the output.

vi) Calculate the ripple factor and efficiency.

vii) Connect the capacitor across the output for each load resistor and measure the output a.c. and d.c. voltages once again and calculate the ripple factor. (If time permits you could also use different values of capacitors and study the output)

Observations:

iv) Code number of diode = _____

v) Input Voltage: V_{ac} =_____Volt

Table(I): Half wave rectifier w/o filter

Sl. No	Load R_L (kΩ)	Output Voltage			Ripple Factor *r*	Efficiency *η* (%)
		V_{ac} (Volt)	V dc (Volt)	V_{max}/π (Volt)		
1						
2						
3						

Table(II): Half wave rectifier with filter (C = ______*μ*F)

Sl. No	Load R_L (kΩ)	Output Voltage		Ripple Factor *r*
		V_{ac} (Volt)	V_{dc} (Volt)	
1				
2				
3				

(III) Input and output waveforms:

Waveforms without Filter: R_L =

_____ **Input** **Output**

(Paste data here)

Waveforms with Capacitor Filter:

R_L = _____ **Input** **Output**

(Paste data here)

3.Characteristics of Zener diode and design a Simple Zener voltage regulator determine line and load regulation

AIM:

To Obtain the Forward Bias and Reverse Bias characteristics of a Zener diode & also find out the Zener Break down Voltage from the Characteristics. And obtain the Load regulation characteristics.

APPARATUS:

S. No.	Name	Range/Value	Quantity
1	DC Regulated Power Supply	0 – 30 volts	1
2	Diode	ECZ 5.1	1
3	Resistor	1K□, 560□	Each 1
4	D.C Ammeters	0–200mA	1
5	D.C Volt meters	0–2V, 0–20V	Each 1
6	Decade Resistance Box	-	1
7	Bread Board and connecting wires	-	1 Set

PROCEDURE:

FORWARD BIAS CHARACTERISTICS:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Switch on the Regulated Power Supply and slowly increase the source voltage. Increase the Diode Current in steps of 2mA and note down the corresponding voltage across the Zener Diode under forward Bias condition as per table given below.
3. Take the readings until a Diode Current of 20mA.
4. Plot the graph V_F versus I_F on the graph Sheet in the 1st quadrant as in Fig.
5. From the graph find out the Static & Dynamic forward Bias resistance of the diode

$$R = \frac{V_F}{I_F}, \qquad r_{ac} = \Delta\frac{V_F}{\Delta I_F}.$$

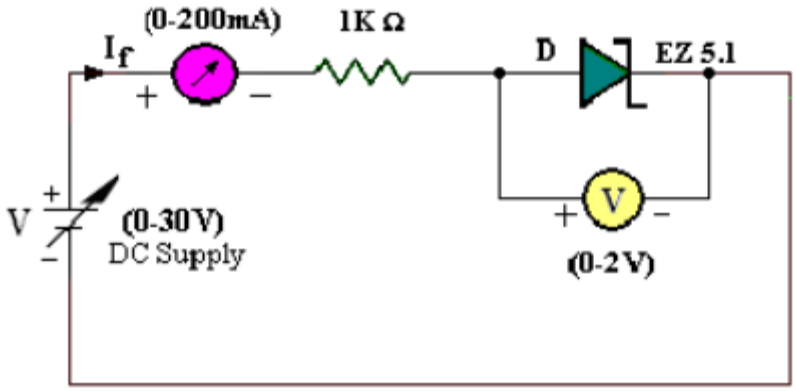
REVERSE BIAS CHARACTERISTICS:

1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. Switch on the Regulated Power Supply and slowly increase the source voltage. Increase the Diode Current in steps of 2mA and note down the corresponding voltage across the Zener Diode under Reverse Bias condition as per table given below.
3. Take the readings until a Diode Current of 20mA.

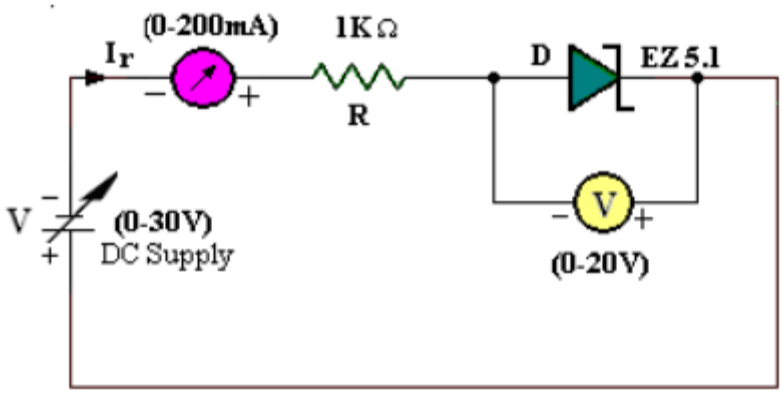
4. Plot the graph V_R versus I_R on the graph Sheet in the 3rd quadrant as in Fig.
5. From the graph find out the Dynamic Reverse Bias resistance of the diode.

   R = $\frac{V_R}{I_R}$, $r_{ac} = \frac{\Delta V_R}{\Delta I_R}$.
6. Observe and note down the break down Voltage of the diode.

CIRCUIT DIAGRAMS:

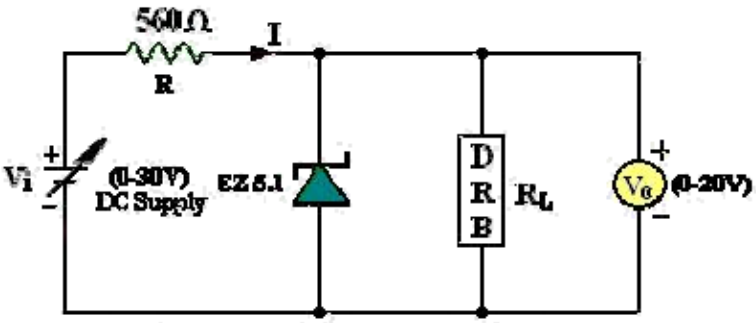


Forward Bias Characteristics



Reverse Bias Characteristics

VOLTAGE REGULATION:



Zener Diode Voltage Regulation

LOAD REGULATION CHARACTERISTICS:

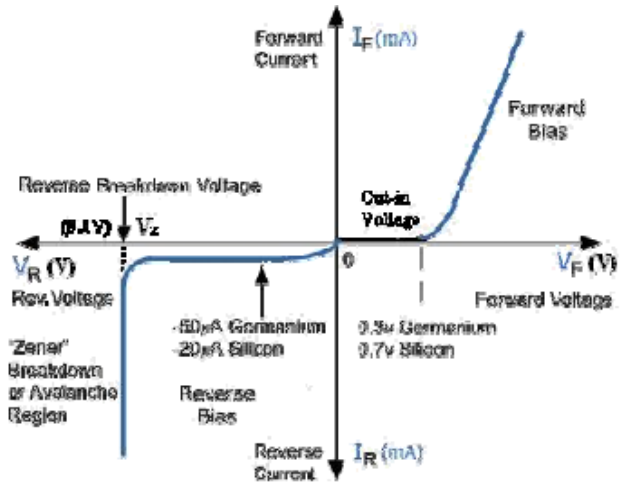
1. Connect the Circuit as per the Circuit Diagram on the bread board.
2. By changing the load Resistance, kept constant I/P Voltage at 5V, 10 V, 15 V as per table given below. Take the readings of O/P Voltmeter (Vo=Vz).
3. Now by changing the I/P Voltage, kept constant load Resistance at 1K, 2K, 3K as per table given below. Take the readings of O/P Voltmeter (Vo=Vz).

ZENER BREAKDOWN VOLTAGE:

Draw a tangent on the reverse Bias Characteristic of the Zener Diode starting from the Knee and touching most of the points of the curve. The point where the tangent intersects the X-axis is the Zener Breakdown Voltage.

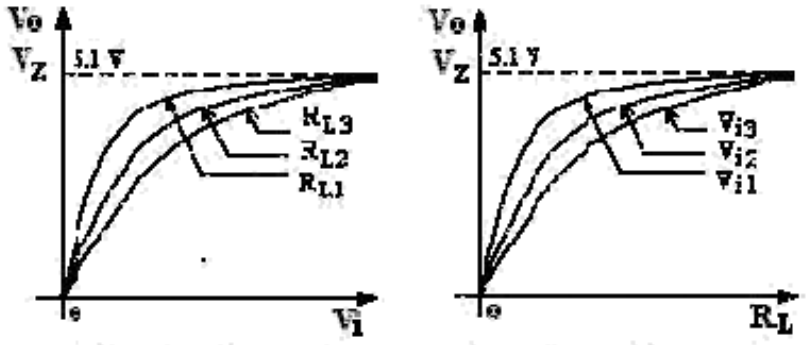
MODEL GRAPHS:

ZENER DIODE CHARACTERISTICS

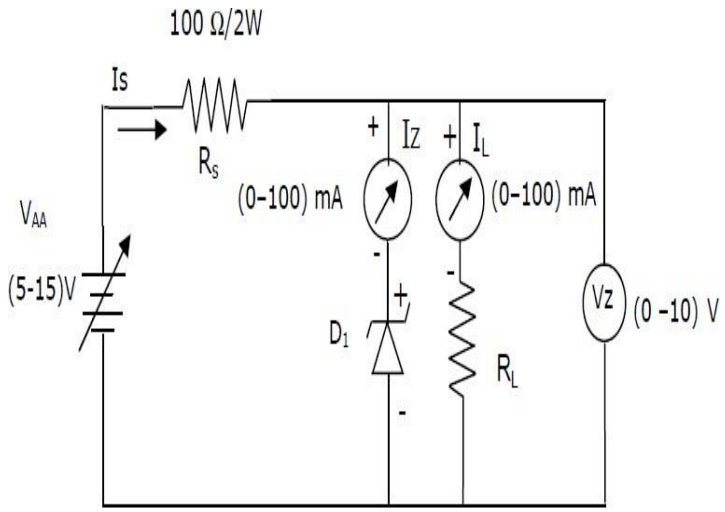


V-I Characteristics of Zener Diode

LOAD REGULATION CHARACTERISTICS:



Voltage Regulation Characstics V_i vs Vo and R_L vs Vo



Line Regulation: Zener Regulator

Regulation with a varying input voltage (line regulation):

It is defined as the change in regulated voltage with respect to variation in line voltage. It is denoted by 'LR'.

In this, input voltage varies but load resistance remains constant hence, the load current remains constant. As the input voltage increases, form equation (3) Is also varies accordingly. Therefore, zener current Iz will increase. The extra voltage is dropped across the Rs. Since, increased Iz will still have a constant Vz and Vz is equal to Vout.

The output voltage will remain constant. If there is decrease in Vin, Iz decreases as load current remains constant and voltage drop across Rs is reduced. But even though Iz may change, Vz remains constant hence, output voltage remains constant.

The input source current, IS = IZ + IL..... (1)

The drop across the series resistance, Rs = Vin – Vz. (2)

And current flowing through it, Is = (Vin – VZ) / RS..... (3)

From equation (1) and (2), we get, (Vin - Vz)/Rs = Iz +IL.....(4)

TABULAR FORMS:

FORWARD BIAS:

S.No	Voltmeter Reading V_F(Volts)	Ammeter Reading I_F (mA)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		

REVERSE BIAS:

Voltmeter Reading V_R (Volts)	Ammeter Reading I_R (mA)

LOAD REGULATION:

S. No	R_L (Ω)	V_{i1}= 5V V_O (V)	V_{i2}= 10V V_O (V)	V_{i3}=15 V V_O (V)
1	100			
2	300			
3	500			
4	700			
5	900			
6	1K			
7	3K			
8	5K			
9	7K			
10	10K			

Vi (V)	R_{L1}=1KΩ V_O (V)	R_{L2}=2KΩ V_O (V)	R_{L3}=3KΩ V_O (V)
0			
1			
3			
5			
7			
9			
11			
13			
15			
20			

RESULT:

The Characteristics of the Forward and Reverse biased Zener Diode and the Zener Break Down Voltage from the Characteristics are Observed.

Zener Breakdown Voltage = Volts.

Forward Bias Resistance = Ohms Reverse Bias Resistance = Ohms

4.Characteristics of LDR and Photo diode and turn on an LED using LDR

Aim:

To plot distance Vs Photocurrent Characteristics of LDR and Photodiode

APPARATUS REQUIRED: **COMPONENTS REQUIRED:**

S. No.	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0–30)mA (0–10)μA		1
3	Voltmeter	(0–10)V		1

S. No.	Name	Range	Type	Qty
1	Photodiod e			1
2	LDR	1K Ω		1 1
3	Bread Board			1
4	Wires			

Theory:

LDR

A photoresistor or light dependent resistor or cadmium sulfide (CdS) cell is a resistor hose resistance decreases with increasing incident light intensity. It can also be referred to as a photoconductor.

A photoresistor is made of a high resistance semiconductor. If light falling on the device is of high enough frequency, photons absorbed by the semiconductor give bound lectrons enough energy to jump into the conduction band. The resulting free electron (and its hole partner) conduct electricity, thereby lowering resistance

Photodiode

A silicon photodiode is a solid state light detector that consists of a shallow diffused PN junction with connections provided to the out side world. When the top surface is illuminated, photons of light penetrate into the silicon to a depth determined by the photon energy and are absorbed by the silicon generating electron-hole pairs.

The electron-hole pairs are free to diffuse (or wander) throughout the bulk of the photodiode until they recombine.

The average time before recombination is the “minority carrier lifetime”.

At the P-N junction is a region of strong electric field called the depletion region. It is formed by the voltage potential that exists at the P-N junction. Those light generated carriers that wander

into contact with this field are swept across the junction.
If an external connection is made to both sides of the junction a photo induced current will flow as long as light falls upon the photodiode. In addition to the photocurrent, a voltage is produced across the diode. In effect, the photodiode functions exactly like a solar cell by generating a current and voltage when exposed to light.

Procedure:

LDR:

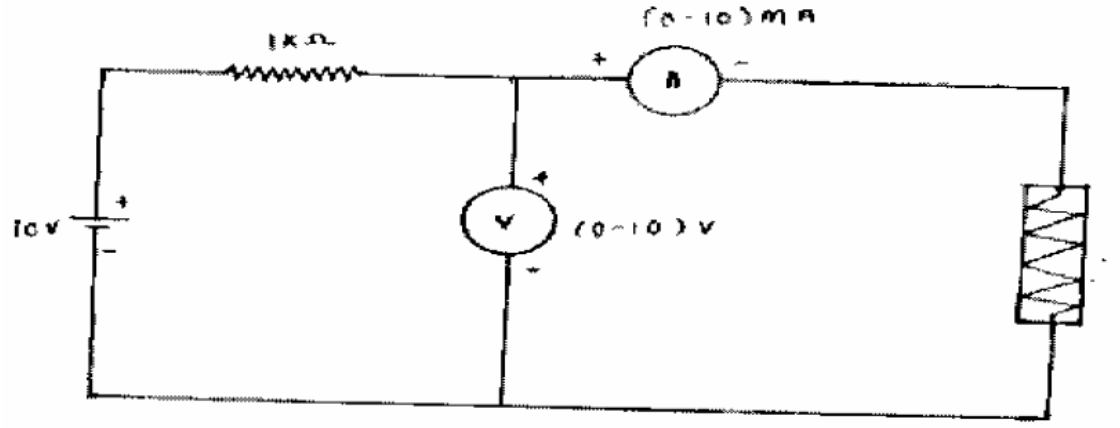
Connect circuit as shown in figure
Keep light source at a distance and switch it ON,so that it falls on the LDR Note down current and voltage in ammeter and voltmeter.
Vary the distance of the light source and note the V & I.
Sketch graph between R as calculated from observed V and I and distance of light source.

Photodiode:

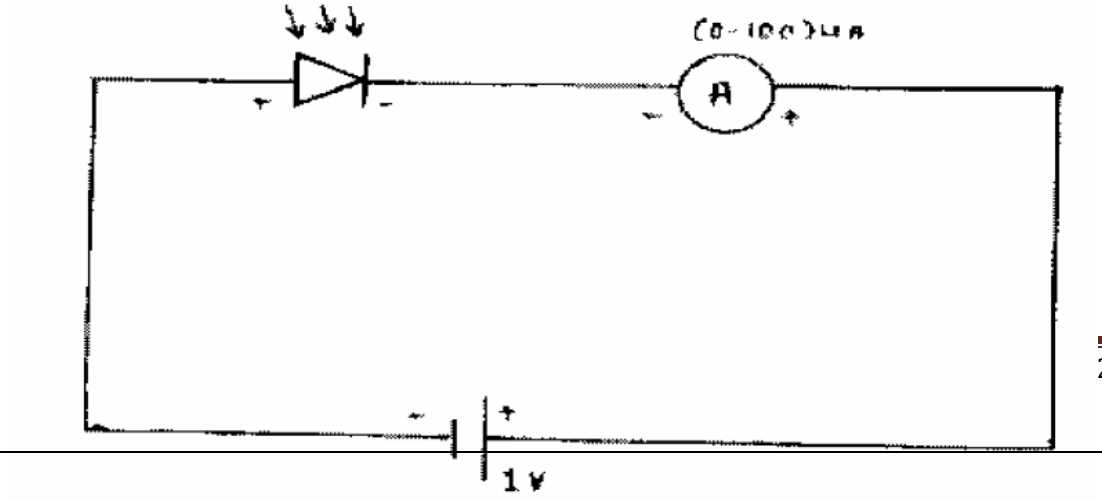
Connect circuit as shown in figure
Maintain a known distance between the bulb and photodiode say 5cm
Set the voltage of the bulb,vary the voltage of the diode in steps of 1 volt and note down the diode current Ir.
Repeat above procedure for VL=4V,6V,etc. Plot the graph :Vd Vs Ir for constant VL

Circuit diagram:

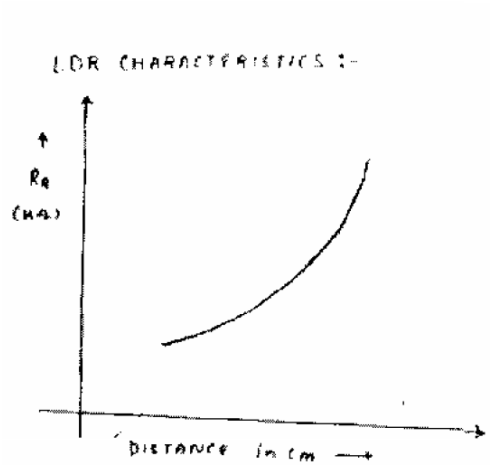
LDR:

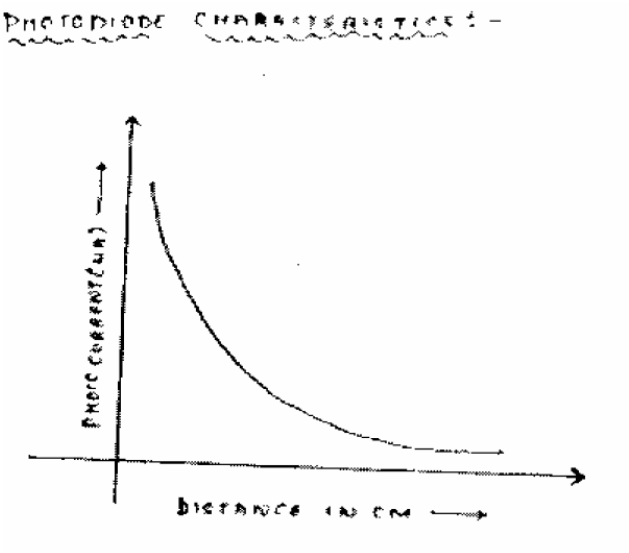


Photodiode:



Graph:


LDR CHARACTERISTICS :-
R_θ
(kΩ)
DISTANCE in cm


DISTANCE IN CM

Tabulation LDR

	Distance (Cm)	Voltage (V)	Current(mA)	R=V/I(Ω)

Photodiode **Distance-constant, VL-Constant**

S. No	VD(V)	IR (mA)

Result:

The characteristics of LDR,Photodiode,Phototransistor is to be tabulated and the graphs are plotted

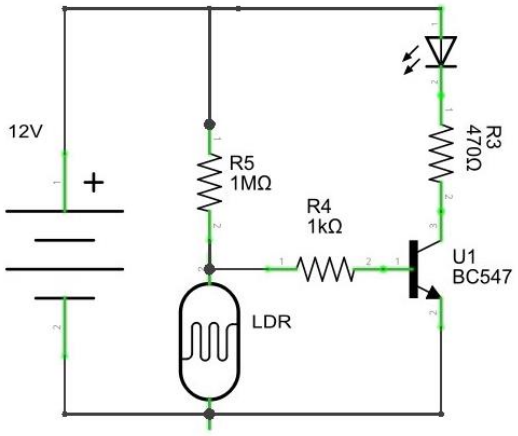
AIM:

To turn on LED using LDR

COMPONENTS REQUIRED

S.NO	NAME	RANGE/VALUE	QUANTITY
1	Transistor	BC547	1
2	Resistor	1MΩ	1
3	Resistor	1KΩ	1
4	Resistor	470Ω	1
5	DC Voltage source	12V	1
6	LDR		1
7	LED		1

CIRCUIT DIAGRAM:



Theory:

LDRs (Light Dependent Resistors): They are also called as photoresistors and photocells. As their names say, they are light dependent (controlled) resistors. The resistance of an LDR decreases with increasing incident light intensity; in other words, it exhibits photoconductivity.

An LDR is made up of a high resistance semiconductor. In the dark it can have a resistance as high as a few megaohms (MΩ), while in the light, it can have a resistance as low as a few hundred ohms. If incident light on an LDR exceeds a certain frequency, photons absorbed by the semiconductor give bound electrons enough energy to jump into the conduction band. The resulting free electrons (and their hole partners) conduct electricity, thereby lowering resistance. The resistance range and sensitivity of a photoresistor can substantially differ among dissimilar devices

A light-emitting diode (LED) is a semiconductor light source that emits light when current flows through it. Electrons in the semiconductor recombine with electron holes, releasing energy in the form of photons. This effect is called electroluminescence. The color of the light (corresponding to the energy of the photons) is determined by the energy required for electrons to cross the band gap of the semiconductor. White light is obtained by using multiple semiconductors or a layer of light-emitting phosphor on the semiconductor device.

PROCEDURE:

To turn on the LED:
1. Connect the circuit as in the circuit diagram.
2. Vary the light intensity falls on LDR.
3. Check whether LED glows.
4. Repeat the experiment for LEDs of different colours.

OBSERVATION:

S.NO	LIGHT FALLS ON LDR	STATUS OF LED
1		
2		

RESULT:
Thus LED control using LDR is observed and verified.

5.Static Characteristics of SCR

Aim:

To obtain static V-I characteristics of SCR for different gate currents and also measure holding current IH, latching current IL and on state resistance of SCR.

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	SCR TYN612	-	1
2.	Resistors	As per design	1 each
3.	Ammeter	0-20/200 mA	2
4.	Multimeter	-	1
5.	Diode BY127	-	1
6.	Transformer	12 – 0 – 12	1
7.	DRB	-	1
8.	CRO Probes	-	1 set

Procedure:

To Plot the V-I Characteristics of SCR:

1. Check the components / Equipment for their workingcondition.
2. Connections are made as shown in the circuit diagram -1.
3. Both RPS-1 and RPS-2 should be in zero position and the supply switch isON
4. To find Gate current required to trigger theSCR:

Fix the anode voltage VAK around 20V (by using the RPS-2). Increase the gate current gradually by using RPS-1 until the SCR turns on (VAK meter becomes approximately0.7V).

5. Bring the RPS-2 to zero position. Now adjust the gate current to the required value by usingRPS-1.
6. Increase the RPS-2 gradually and the corresponding readings of V_{AK} and I_A are noted down.
7. When RPS-2 reaches a particular value, SCR turns on for the second time. Notedown that RPS-2 value i.e the break overvoltage.
8. Repeat the steps 6 and 7 for some other gate currentvalue.
9. Graph between V_{AK} and I_A isplotted.

To find the Holding Current (I_H):

1. Connections are made as shown in the circuitdiagram-1.
2. Keep the anode voltage around 20V by using RPS-2 and turn on the SCR by applying the required gate current by usingRPS-1.
3. Bring back RPS-1 to zero position and switch off.

4. Gradually reduce the anode voltage by using RPS-2. Anode current also decreases slowly, at certain value, the anode current will jumps to zero suddenly. Note down this current value. (This is Holding Current).

To find the Latching Current (I_L):

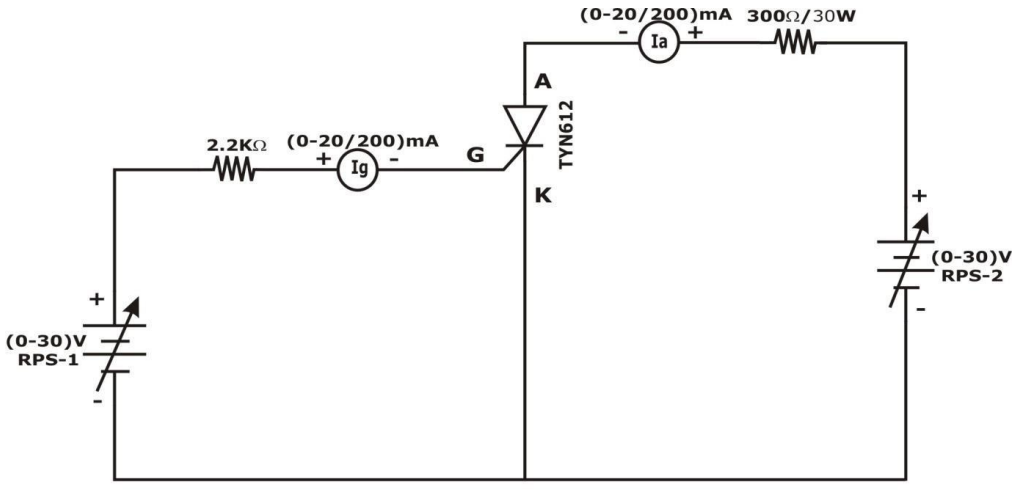
1. Connections are made as shown in the circuitdiagram-2.
2. Keep DRB in maximum resistance position
3. Apply the VAA around 20V by using RPS
4. Observe the square waveform across the anode and cathode of SCR (now SCR is operating in Gate dependent mode)
5. Now reduce the DRB (from higher range to lower) gradually till the square wave disappears (now SCR is operating in Gate independent mode)
6. Note down the anode current at which the square wave disappear (This is Latching Current)

Calculation:

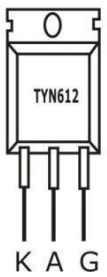
On state resistance $R_{on} = \Delta V_{AK}/\Delta I_A =$ _____ Ω

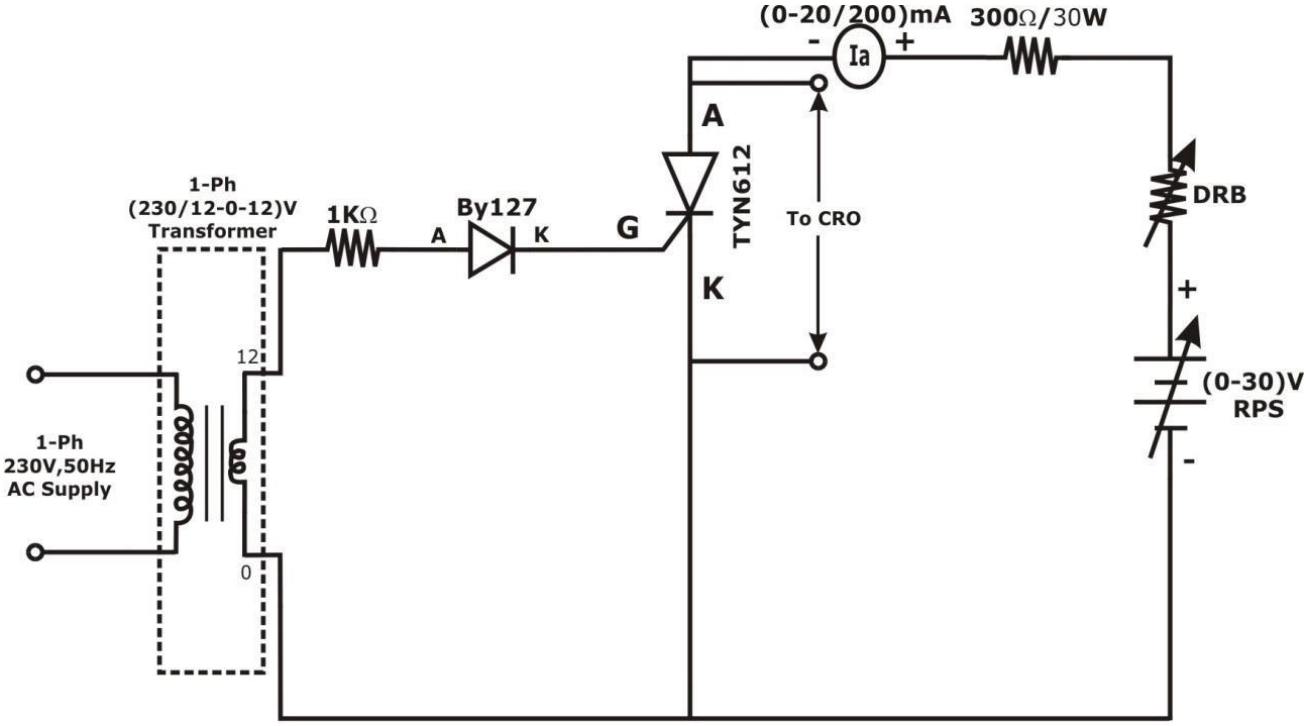
Design:

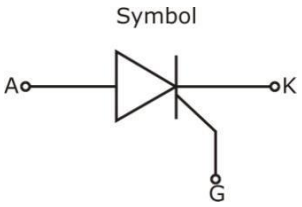
$V_{AK} = V_{AA} - I_A R_A$
$R_A = (V_{AA} - V_{AK}) / I_A$
Assume $V_{AAmax} = 30$ V, $V_{AKon} = 0.7$ V, and $I_A = 100$ mA
Then $R_A = 293\ \Omega$ choose $R_A = 300\ \Omega$
and $P_{RA} = (V_{AAmax} - V_{AKon})^2 / R_A = 2.86$ W
Therefore $R_A = 300\ \Omega$ / 10 W



Pin Diagram




(0-20/200)mA
300Ω/30W
-
Ia
+
A
TYN612
G
K
To CRO
DRB
+
(0-30)V
RPS
-
1-Ph
(230/12-0-12)V
Transformer
1KΩ
By127
A
K
12
0
1-Ph
230V,50Hz
AC Supply


Symbol
A
K
G

Tabular Column:

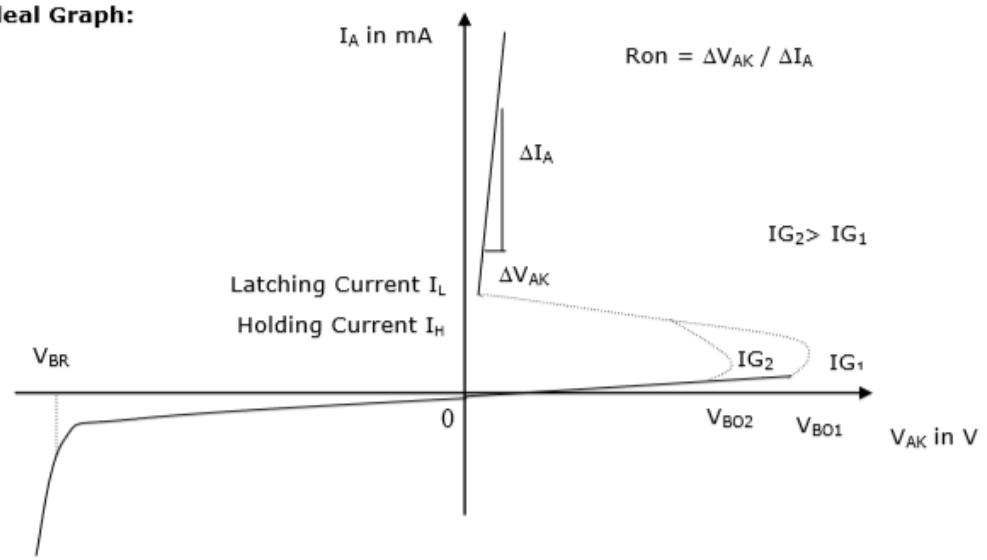
IG_1=_____mA, V_{BO1}=_____V

IG_2=_____mA,V_{BO2}=_____V

V_{AK} in Volts	I_A in mA

V_{AK} in Volts	I_A in mA

Ideal Graph:



Result:

The on state resistance of SCR R_{on} =_____Ω

The holding current I_H=_____

_____mA

The latching current I_L=_____mA

At gate current

I_{G1}=___mA

the break over voltageV_{BO1}=.V I_{G2}=.mA

the break over voltageV_{BO2}=.V

6. SCR Controlled HWR and FWR using RC triggering circuit

Aim:

To study the performance & waveforms of HWR & FWR by using RC triggering Circuit.

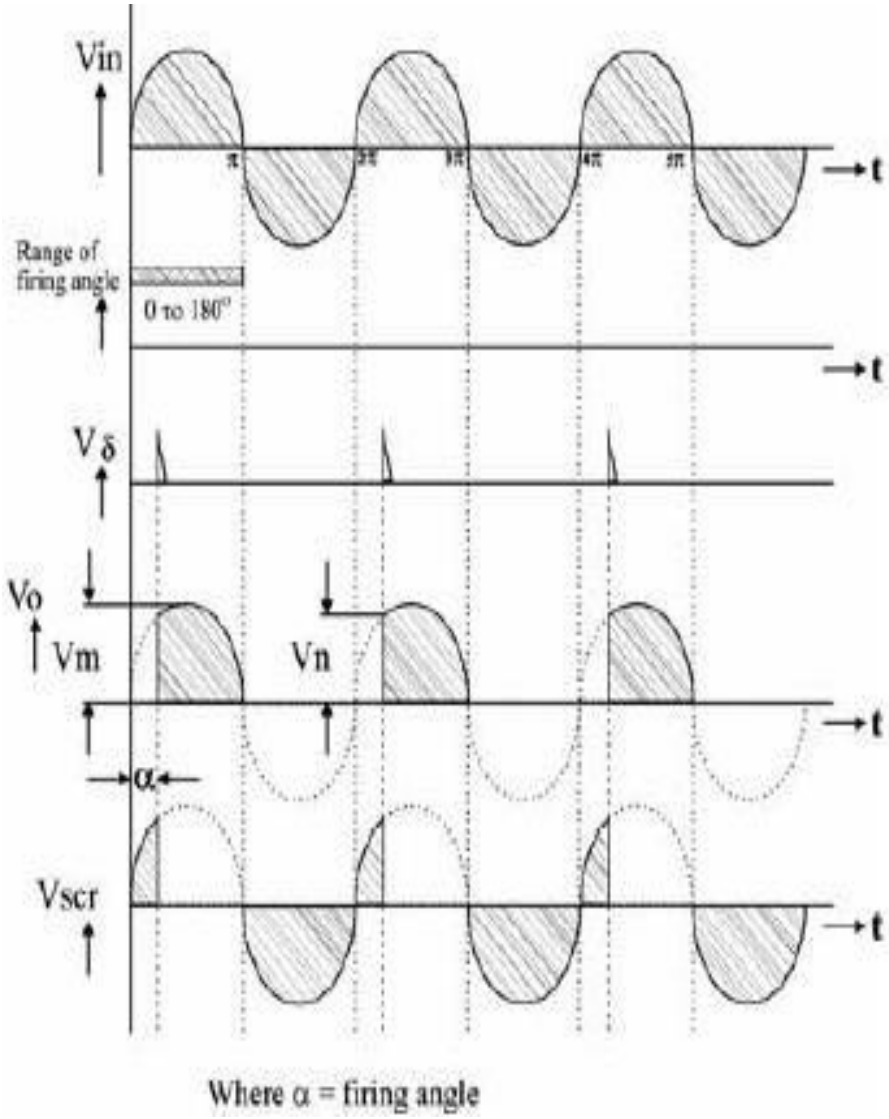
Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	SCR – TYN612	-	1
2.	Transformer	230/12-0-12 V	1
3.	CRO Probe	-	1 set
4.	Diode- BY127		1
5.	Resistor	-	2
6.	DRB,DCB		1

Procedure:

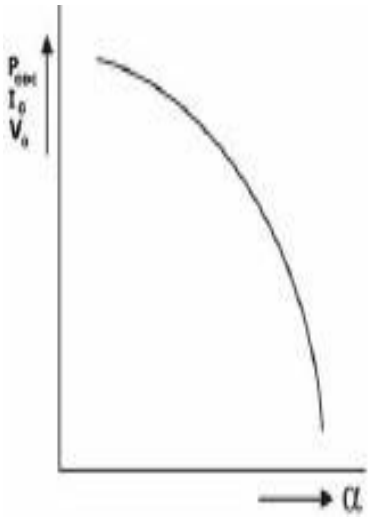
1. Connections are made as shown in circuitdiagram-6,7.
2. Keep the value of DRB at 1K and DCB at 0.1uf. Switch ON thesupply.
3. Now vary the firing angle by increase the value of resistance in DRB in steps, observe the waveforms and note down the corresponding values of V_n and $V_m$from CRO and $V_{odc}$from the DC voltmeter. The readings are tabulated in the tabularcolumn.
4. If the firing angle ranges from 0 to 90º, then the firing angle α is calculated by using formula $\alpha = \sin^{-1}(V_n/V_m)$ indegrees.
5. The conduction angle β is calculated using the formula, β =180-α.
6. Thecurrentandpoweriscalculatedby$I_{odc}=V_{odc}$/RampereandP$_{odc}=V^2$ /RWatts odc respectively .
7. A graph of V_o v/s α, V_o v/s β, I_o v/s α, I_o v/s β, P_{odc}v/s α and P_{odc}v/s β are to beplotted.
8. Compare the practical output voltage with the theoretical output voltage, () () V. Where $V_m = \sqrt{2}*V_{rms}$.

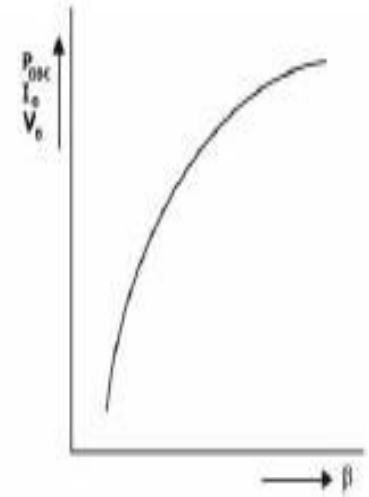
Waveforms:



Where α = firing angle

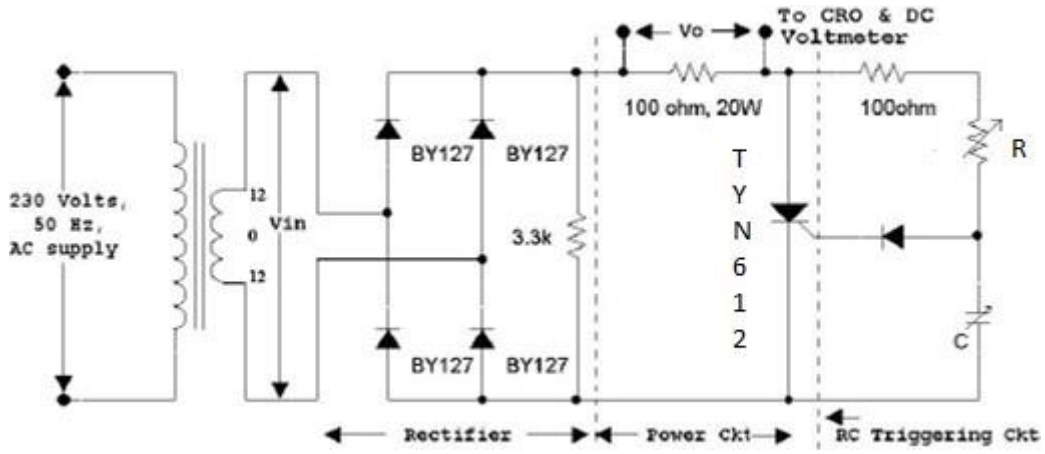
Graph:





Full Wave Rectifier using RC Triggering

Circuit diagram



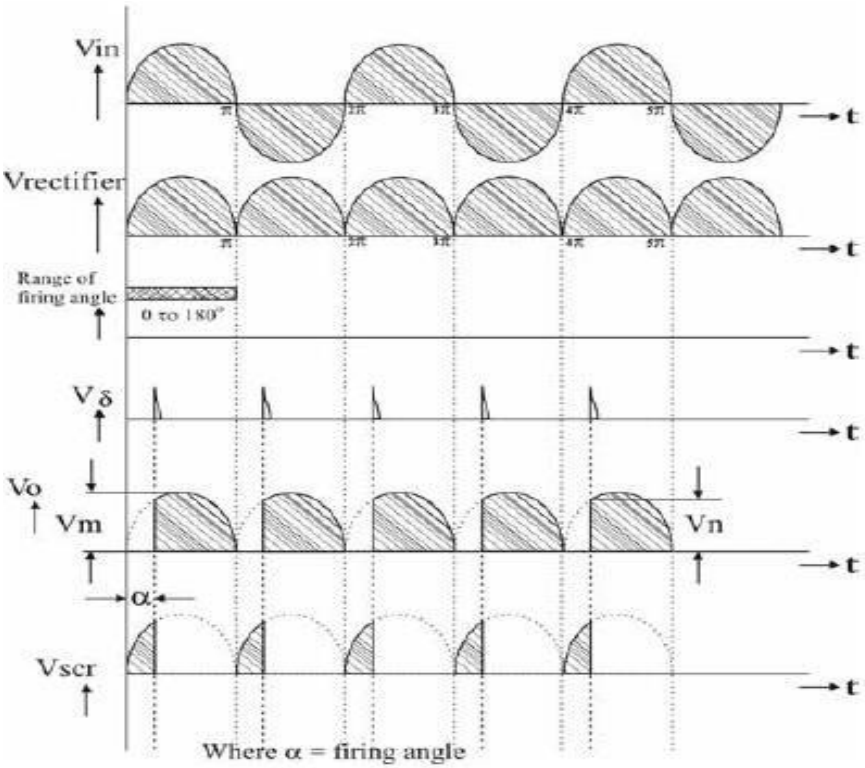
Design:

$RC \geq 50/2f$

$$R_{max} \leq \frac{Vs - Vgt}{Igt(\min)} = \frac{24\sqrt{2} - 1.3}{2mA} = 16.32k\Omega$$

$$R_{min} \leq \frac{Vs - Vgt}{Igt(\max)} = \frac{24\sqrt{2} - 1.3}{25mA} = 1.3k\Omega$$

Waveform:


Vin
Vrectifier
Range of
firing angle
0 to 180°
Vδ
Vo
Vm
Vn
α
Vscr
t
Where α = firing angle

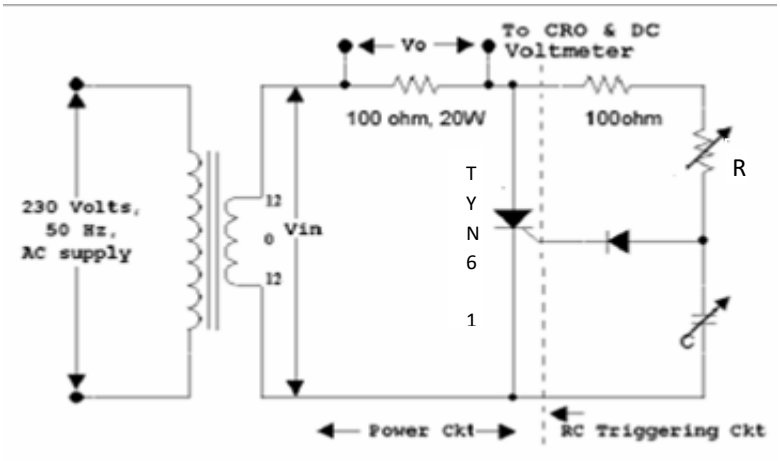
Tabular Columns:

FullWaveRectifier: V_m=_____V

		α<90°	α>90°		
	V_n	() —	() —	V_{odc}	V_{oth}

Half Wave Rectifier using RC Triggering

Circuit diagram:



Design:

$$RC \geq \frac{1.3T}{2}$$

The SCR will turn ON only when

Capacitor voltage : $V_C = V_{g(min)} + V_{D1}$

Transformer Secondary : $V_S \geq I_{g(min)}R + V_c$

$$\therefore \quad V_S \geq I_{g(min)}R + V_c$$

$$\geq I_{g(min)}R + V_{g(min)} + V_{D1}$$

$$R \leq \frac{V_s - V_{g(min)} - V_{D1}}{I_{g(min)}}$$

From the data sheet of TYN612, $V_{g(min)} = 1.3V$, $V_{D1} = 0.7V$, $I_{g(min)} = 2mA$, $I_{g(max)} = 25mA$

$$\therefore R_{(min)} = \frac{24\sqrt{2} - 1.3 - 0.7}{I_{gt(max)}} = \frac{31.9}{25mA} = 1.277k\Omega$$

$$R_{(max)} = \frac{24\sqrt{2} - 1.3 - 0.7}{2mA} = 16k\Omega$$

HalfWaveRectifier: V_m=_____V

	V_n	α<90º	α>90º	V_{odc}	V_{oth}
		()	()		

7. Conduct an experiment to measure temperature in terms of current/voltage using a temperature sensor bridge

Aim:

To detect the small variations of resistance of the RTD, a temperature transmitter in the form of a Wheatstone bridge is generally used. The circuit compares the RTD value with three known and highly accurate resistors.

Apparatus:

Theory:

The change in the resistance of metals with temperature provides the basic for a family of temperature measuring sensors known as resistance temperature detectors. The sensor is simply a conductor fabricated either as a wire would coil or as a film or foil grid. The change in resistance of the conductor with temperature is given by the expression.

$\Delta R / R_0 = \lambda_1 (T-T_0) + \lambda_2 (T-T_0)^2 + \lambda_n (T-T_0)^n$

Where T_0 is a referencetemperature.

R_0 is the resistance at temperature T_0

$\lambda_1, \lambda_2, \ldots\ldots\ldots\ldots \lambda_n$ are temperature co-efficient of resistance.

Platinum is widely used for sensor fabrication since it is the most stable of all the metals, is the least sensitive to contamination, and is capable of operating over a very wide range of temperature. The dynamic response of on RTD depends almost entirely on construction details.

This bridge is used to find the unknown resistance very precisely by comparing it with a known value of resistances. In this bridge null or balanced condition is used to find the resistance.

For this bridge balanced condition voltage at points C and D must be equal. Hence, no current flows through the galvanometer. For getting the balanced condition one of the resistors must be variable.

From the figure,

The voltage at point $\mathbf{D = V \times R_X / (R_3 + R_X)}$

The voltage at point $\mathbf{C = V \times R_2 / (R_1 + R_2)}$

The voltage (V) across galvanometer or between C and D is,

$\mathbf{V_{CD} = V \times R_X / (R_3 + R_X) - V R_2 / (R_1 + R_2)}$

When the bridge is balanced $V_{CD} = 0$,

So,

$\mathbf{V \times R_X / (R_3 + R_X) = V R_2 / (R_1 + R_2)}$

$\mathbf{R_X R_1 + R_X R_2 = R_2 R_3 + R_2 R_X}$

$\mathbf{R_1 R_X = R_2 R_3}$

$\mathbf{R_2/R_1 = R_X/R_3}$

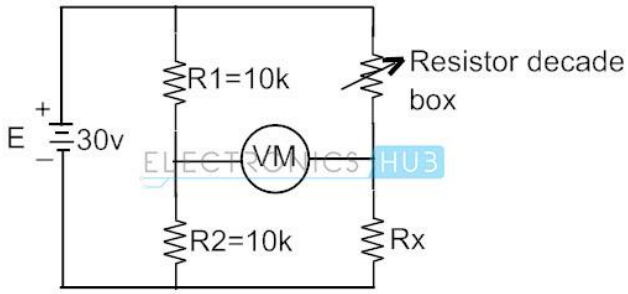
This is the condition to balance the bridge. And for finding the unknown value of resistance

$\mathbf{R_X = R_3 \times (R_2 / R_1)}$

From the above equation R4 or Rx can be computed from the known value of resistance R3 and the ratio of R2/R1. Therefore, most of the cases R2 and R1 values are fixed and the R3 value is variable so that null value is achieved and the bridge gets balanced.

From above, the Wheatstone bridge is unbalanced when the voltmeter reading is not zero. This reading can be positive or negative depends on the magnitudes of the voltages at the

meter terminals. Let us consider the below circuit of Wheatstone bridge which is connected to find the unknown resistance value with use of resistor decade box to get the variable resistance of R_3.



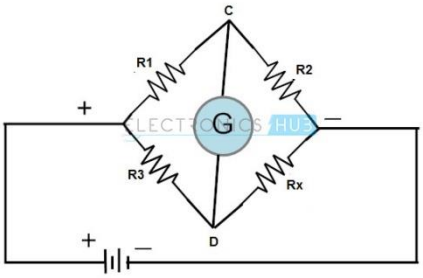
We know that the condition for bridge balance is

$R_4 = R_3 \times R_2 / R_1$

$R_x = R_{BOX} \times (10 \times 10^3) / (10 \times 10^3)$

$R_x = R_{BOX}$

Here in this case, the Wheatstone bridge is balanced by adjusting the decade resistance box until the voltmeter reads zero value. And the corresponding resistance value in the box is equal to the unknown resistance. Suppose if the voltage null condition occurs at 250 ohms of the resistance decade box, then the unknown resistance is also 250 ohms.



8.Measurement of Resistance using Wheatstone and Kelvin's bridge

AIM:

To measure the given medium resistance using Wheatstone bridge.

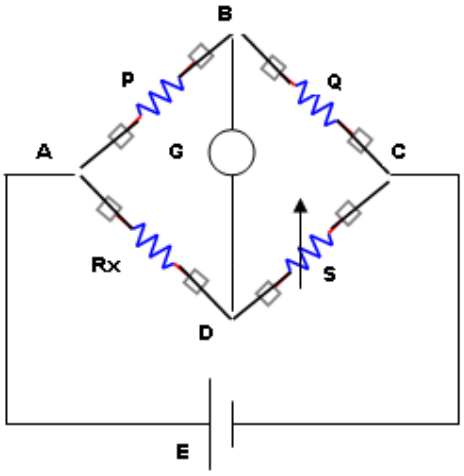
OBJECTIVE:

To study the working of bridge under balanced and unbalanced condition and to study the sensitivity of bridge.

APPARATUS REQUIRED:

SL. NO	NAME OF THE APPRATUS	RANGE	TYPE	QTY
1 2 3 4	Wheat stone Bridge kit Unknown resistance Multimeter Connecting Wires.			

CIRCUIT DIAGRAM:



THEORY:

The change in the resistance of metals with temperature provides the basic for a family of temperature measuring sensors known as resistance temperature detectors. The sensor is simply a conductor fabricated either as a wire would coil or as a film or foil grid. The change in resistance of the conductor with temperature is given by the expression.

$\Delta R / R_0 = \lambda_1 (T-T_0) + \lambda_2 (T-T_0)^2 + \lambda_n (T-T_0)^n$

Where T_0 is a reference temperature.

R_0 is the resistance at temperature T_0

$\lambda_1, \lambda_2, \ldots\ldots\ldots\ldots \lambda_n$ are temperature co-efficient of resistance.

Platinum is widely used for sensor fabrication since it is the most stable of all the metals, is the least sensitive to contamination, and is capable of operating over a very wide range of temperature. The dynamic response of on RTD depends almost entirely on construction details.

This bridge is used to find the unknown resistance very precisely by comparing it with a known value of resistances. In this bridge null or balanced condition is used to find the resistance.

For this bridge balanced condition voltage at points C and D must be equal. Hence, no current flows through the galvanometer. For getting the balanced condition one of the resistors must be variable

FORMULAE USED:

Unknown Resistance, $R_x = (P/Q)\ S\ (\Omega)$

Where P, Q = Ratio Arms.

S = Variable resistance,

R_x = Unknown resistance.

PROCEDURE:

1. The resistance to be measured is connected between XX points in the bridge kit.
2. The P/Q ratio (multiplier) is initially kept at position '1' and the deflection of the galvanometer is observed by pressing both the battery and the galvanometer keys.
3. The S arm (X 1000Ω) is adjusted and two positions are identified for which the deflection of the galvanometer is on either side of the null point and kept at the lowest value of S. Then the x100Ω, x10Ω, x1Ω knobs of S are adjusted to get null deflection. If necessary the sensitivity knob may be adjusted to get appreciable deflection. [If not possible P/Q ratio is kept at any other suitable value ie, any one of ratios provided.]
4. The value of unknown resistance is read. (S value)
5. Steps 3 and 4 are repeated for some other P/Q ratio. The mean value is taken.
6. The experiment is repeated with other samples provided.

NOTE: The above experiment may be used for measuring resistance of the samples less than 1Ω to greater than 10kΩ with lesser sensitivity.

TABULAR COLUMN:

S.NO	SAMPLE	P/Q RATIO (MULTIPLIER)	S VALUE (Ω)	UNKNOWN RESISTANCE R_X (Ω)

RESULT:

MEASUREMENT OF RESISTANCE USING KELVIN'S DOUBLE BRIDGE.

AIM:

To measure the given low resistance using Kelvin's double bridge method.

OBJECTIVE

1. To study the working of bridge under balanced and unbalance condition.
2. To study the sensitivity of bridge.

EQUIPMENT

1. Kelvin Double bridge kit – 1 No
2. Unknown resistance – 1 No
3. Multimeter – 1 No
4. Connecting wires.

FORMULA USED:

Rx=P/Q * S ohms Where

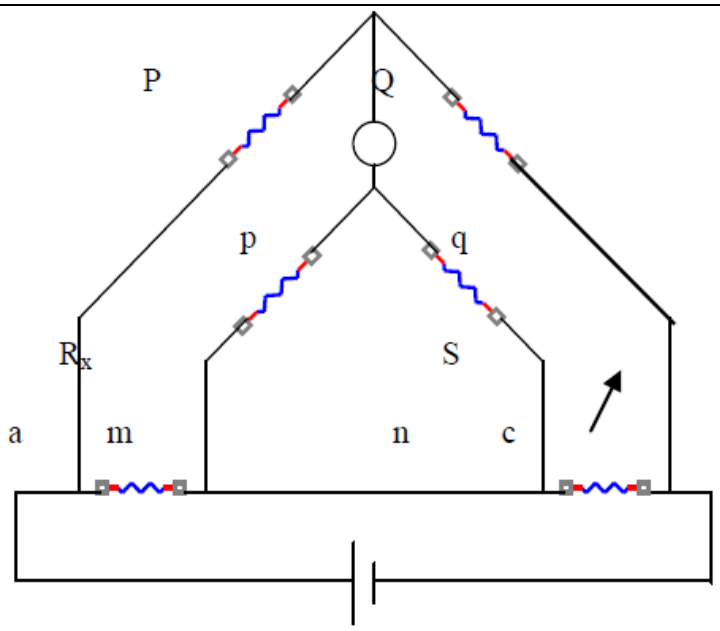
EXERCISE

1. Design a bridge for the given parameters.
2. Find the unknown low resistance.
3. Find the sensitivity of bridge

PROCEDURE:

1. The resistance to be measured is connected such that the leads from +C and + P are connected to one end and those
   From –C and –P are connected to the other end in the kit.
2. The P/Q ratio (multiplier) is initially kept at position '1' and the deflection of the galvanometer is observed by
   Pressing the galvanometer key.
3. The 'S' arm (main dial) is adjusted and two positions are identified for which the deflection o f the galvanometer is
   On either side of the null point. [If not some other P/Q ratio is to be tried].
4. The lower of the two positions indicates the coarse value of the unknown resistance and the null point is obtained by
   Adjusting the Vernier scale, with the galvanometer sensitivity knob at the maximum position.
5. The value of unknown resistance is read. ['S' Value]
6. Steps 3,4,5 are repeated for some other P/Q ratio for the unknown resistance. The mean value is taken.
7. The above procedure is repeated with another sample.

CIRCUIT DIAGRAM



TABULAR COLUMN:

S.NO	SAMPLE	P/Q RATIO (Multiplier)	S VALUE		UNKNOWN RESISTANCE RX (Ω)
			COARSE (Ω)	FINE (Ω	

RESULT:

The value of unknown resistan

PART B (Simulation)

9.Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters

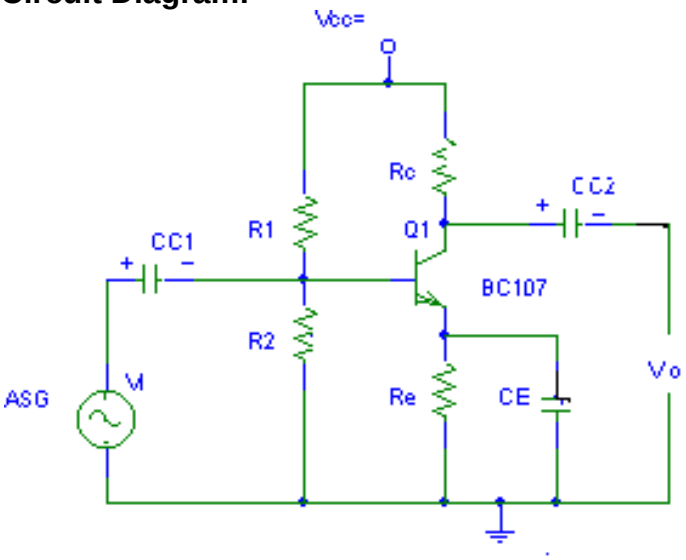
Aim : To design and set up the common emitter amplifier under voltage divider bias with and without feedback and determine the gainbandwidth product from its frequency response.

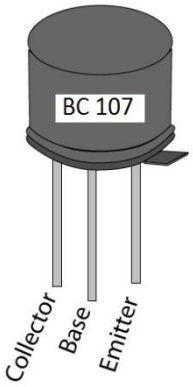
Components required:

Sl no.	Components required	Range	Qty
1.	Transistor(BJT)	BC107	1
2.	Resistors(for BJT)	18KΩ, 82KΩ, 1KΩ, 3.9KΩ	1 each
3.	Capacitors	1µF (3 nos)	1 each
4.	CRO		1
5.	Power supply(VRPS)	0-30 V	1each
6.	ASG		1
7.	DRB		1

a) To find gain and frequency response of CE amplifier without feedback using BJT.

Circuit Diagram:





$R_1 = 82K\Omega,$
$R_2 = 18K\Omega$
$R_C = 3.9K\Omega$
$R_E = 1K\Omega$
$C_E = 10\mu F$
$C_C = 1\mu F$
$V_{CC} = 10V$

Design :

Design RC coupled amplifier for V_{CC} = 10V, h_{fe} = 100, I_C = 1mA, V_{CE} = 5 V.

$$I_b = \frac{I_c}{h_{fe}} = 0.01mA$$

$$I_E = I_C + I_B = 1.01mA$$

For a voltage divider bias,

$$V_E = \frac{V_{CC}}{10} = 1V$$

$$R_E = \frac{V_E}{I_E} = \frac{1V}{1.01mA} = 990\Omega \cong 1k\Omega$$ (Choose 1 KΩ)

This can also be synthesized as a series of 470Ω and 1K pot.

$$V_B = V_E + V_{BE} = 1 + 0.7 = 1.7V$$

In a voltage divider bias,

$$V_{R2} = I_2 R_2 = V_E + V_{BE}$$

$$I_2 = 10 I_B$$

$$\therefore R_2 = \frac{V_E + V_{BE}}{10 I_B} = 17k\Omega \cong 18k\Omega$$

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$R_1 = 87.8k\Omega \cong 82k\Omega$$

$$R_C = \frac{V_{CC} - V_E - V_{CE}}{I_C} = 4k\Omega$$

To find C_E and Cc:

$$X_{CE} = \frac{R_E}{10}$$

$$\frac{1}{2\pi f C_E} = \frac{R_E}{10}$$

$$f = 100Hz, C_E = \frac{10}{2\pi f R_E} = 15\mu F \cong 10\mu F$$

Coupling Capacitor C_c = $C_C = \frac{1}{2\pi f_L R_i} \cong 1\mu F$

$$R_i = R_1 \| R_2 \| (1 + h_{fe}) r_e$$ where $r_e = \frac{26mV}{I_E} = 24.7\Omega$

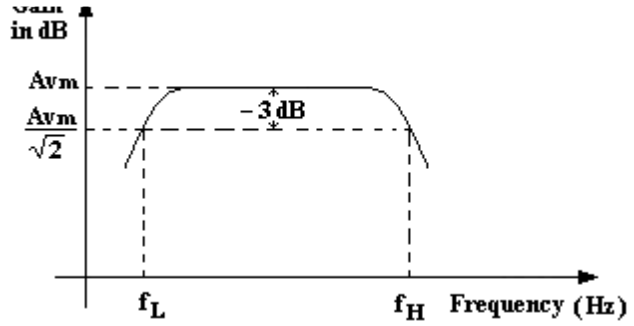
Procedure :

- Connections are made as shown in the circuit diagram and set Vcc =10V
- Measure the dc voltage at V_B , collector V_C ,emitter V_E w.r.t ground.. Determine V_{CE} & I_C. ∴Operating point (Q) = (V_{CE} , I_C) = (5V ,1mA)
- For the circuit connected apply the sinusoidal wave of peak to peak amplitude 20mV from the signal generator.
- Vary the frequency of the input signal(from 100Hz to 1MHz) in suitable steps and Measure the output of the amplifier at each step using CRO (input V_i must remain constant throughout the frequency range) and Record the results in tabular column. Calculate the voltage gain.
- Plot the graph of frequency vs voltage gain in dB on a semilog graph sheet.
- Calculate the bandwidth = upper cutoff (f_2) – lower cutoff (f_1)

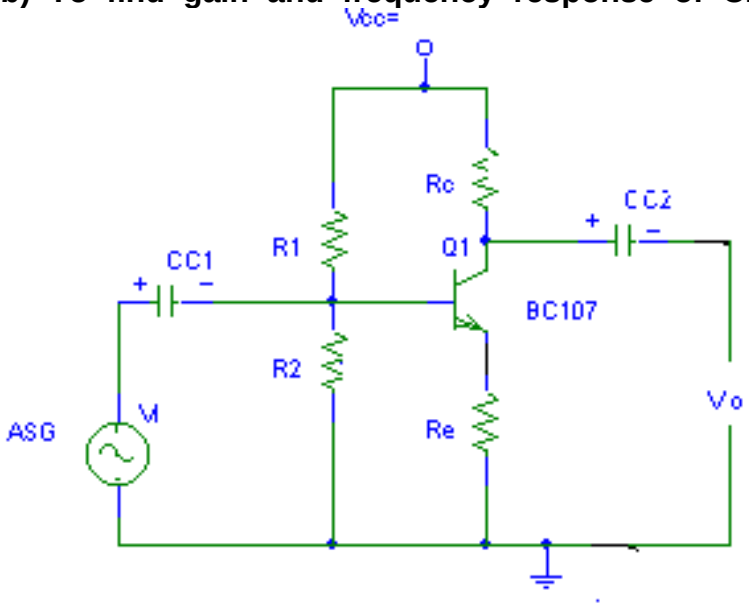
Tabular Column :

Freq (Hz)	V_o (V)	V_o/V_i	A_v(dB)= 20 log(V_o/V_i)

Expected Graph:



b) To find gain and frequency response of CE amplifier with feedback using BJT



$R_1 = 82K\Omega,$
$R_2 = 18K\Omega$
$R_C = 3.9K\Omega$
$R_E = 1K\Omega$
$C_E = 10\mu F$
$C_C = 1\mu F$
$V_{CC} = 10V$

Note: Repeat the same procedure followed for the CE amplifier without feedback using BJT, and determine the gain bandwidth product for CE amplifier with feedback.

Tabular Column:

Freq (Hz)	V_o (V)	V_o/V_i	A_v(dB)= 20 log(V_o/V_i)

Result :

Sl.No	Details	Without Feedback	With Feedback
1	Operating Point		
2	Gain in db		
3	Bandwidth		
4	Gain – Bandwidth product		

10.Transfer and drain characteristics of a JFET and MOSFET.

Aim: To plot the input and output characteristics of a JFET and calculate its parameters, namely; drain dynamic resistance, mutual conductance and amplification factor.

Objective:

To study Drain Characteristics and Transfer Characteristics of a Field Effect Transistor (FET).

Components:

S.No.	Name	Quantity
1	JFET (BFW11/ BFW10)	1(One) No.
2	Resistor (1KΩ ,100KΩ)	1(One) No. Each
3	Bread board	1(One) No.

Equipment:

S.No.	Name	Quantity
1	Dual DC Regulated Power supply (0 - 30 V)	1(One) No.
2	Digital Ammeters (0 - 200 mA)	1(One) No.
3	Digital Voltmeter (0 - 20V)	2(Two) No.
4	Connecting wires (Single Strand)	

Specifications:

For FET BFW11:

- Gate Source Voltage V_{GS} = -30V
- Forward Gain Current I_{GF} = 10mA
- Maximum Power Dissipation P_D = 300mW

Circuit Diagram:

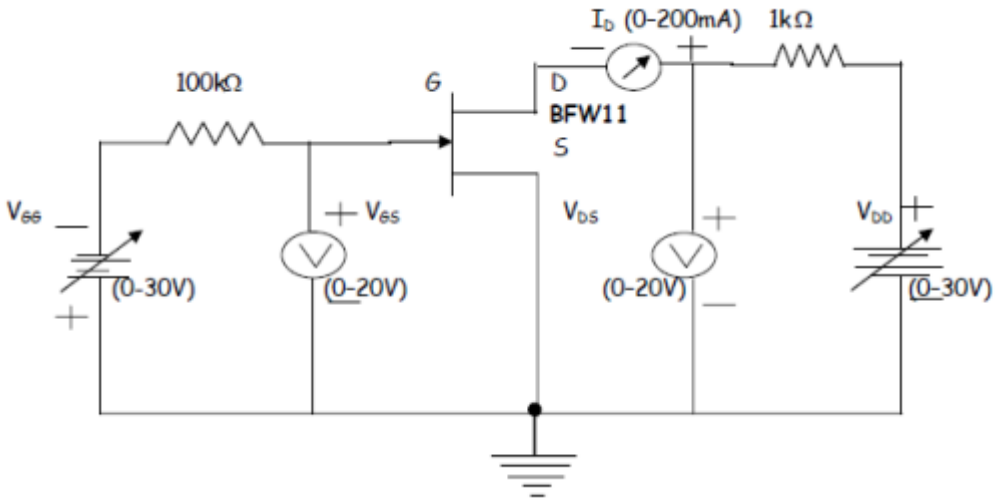
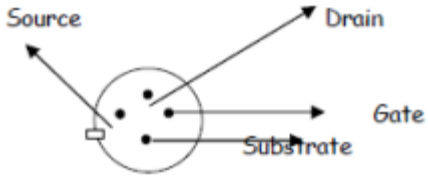
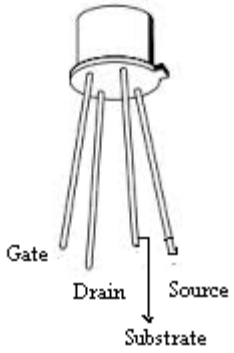


Figure 1.

Pin assignment of FET:



Top View



Bottom View

Operation:

The circuit diagram for studying drain and transfer characteristics is shown in the figure1.

1. Drain characteristics are obtained between the drain to source voltage (V_{DS}) and drain current (I_D) taking gate to source voltage (V_{GS}) as the constant parameter.
2. Transfer characteristics are obtained between the gate to source voltage (V_{GS}) and drain current (I_D) taking drain to source voltage (V_{DS}) as the constant parameter.

Procedure:

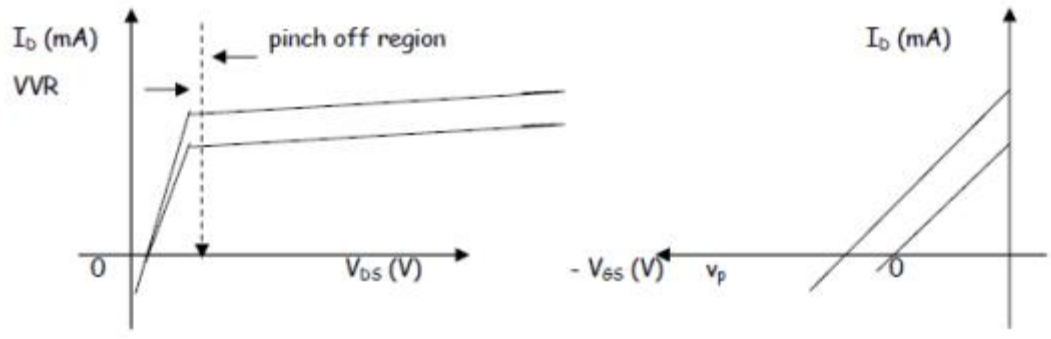
Drain Characteristics:

1. Connect the circuit as shown in the figure1.
2. Keep $V_{GS} = 0V$ by varying V_{GG}.
3. Varying V_{DD} gradually in steps of **1V** up to **10V** note down drain current I_D and drain to source voltage (V_{DS}).
4. Repeat above procedure for $V_{GS} = -1V$.

Transfer Characteristics:

1. Connect the circuit as shown in the figure1.
2. Set voltage $V_{DS} = 2V/5V$ (BFW10/ BFW11).
3. Varying V_{DD} in steps of 0.5V until the current I_D reduces to minimum value.
4. Varying V_{GG} gradually, note down both drain current I_D and gate-source voltage(V_{GS}).
5. Repeat above procedure (step 3) for V_{DS} = 4V/ 8V (BFW10/ BFW11).

Graph:



DRAIN CHARACTERISTICS TRANSFER CHARACTERISTICS

1. Plot the drain characteristics by taking **V_{DS}** on X-axis and **I_D** on Y-axis at a constant **V_{GS}**.
2. Plot the transfer characteristics by taking **V_{GS}** on X-axis and taking **I_D** on Y-axis at constant **V_{DS}**.

Calculations from Graph:

1. **Drain Resistance (r_d):** It is given by the relation of small change in drain to source voltage(ΔV_{DS}) to the corresponding change in Drain Current(ΔI_D) for a constant gate to source voltage (ΔV_{GS}), when the JFET is operating in pinch-off region.

   $$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$ at a constant **V_{GS}** (from drain characteristics)

2. **Trans Conductance (g_m):** Ratio of small change in drain current(ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant **V_{DS}**.

   g_m $= \frac{\Delta I_D}{\Delta V_{GS}}$ at constant **V_{DS}** (from transfer characteristics).

   The value of **g_m** is expressed in mho's ($\mho$) or Siemens (**S**).

3. **Amplification factor (μ):** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).

   $$\mu = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) * \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) = \frac{\Delta V_{DS}}{\Delta V_{GS}} = r_d * gm$$

Inference:

1. As the gate to source voltage (**V_{GS}**) is increased above zero, pinch off voltage is increased at a smaller value of drain current as compared to that when **V_{GS} = 0V**.
2. The value of drain to source voltage (**V_{DS}**) is decreased as compared to that when **V_{GS} = 0V**.

Precautions:

1. While performing the experiment do not exceed the ratings of the FET. This may lead to damage of FET.
2. Connect voltmeter and ammeter with correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless the circuit connections are checked as per the circuit diagram.
4. Properly identify the Source, Drain and Gate terminals of the transistor.

Result:

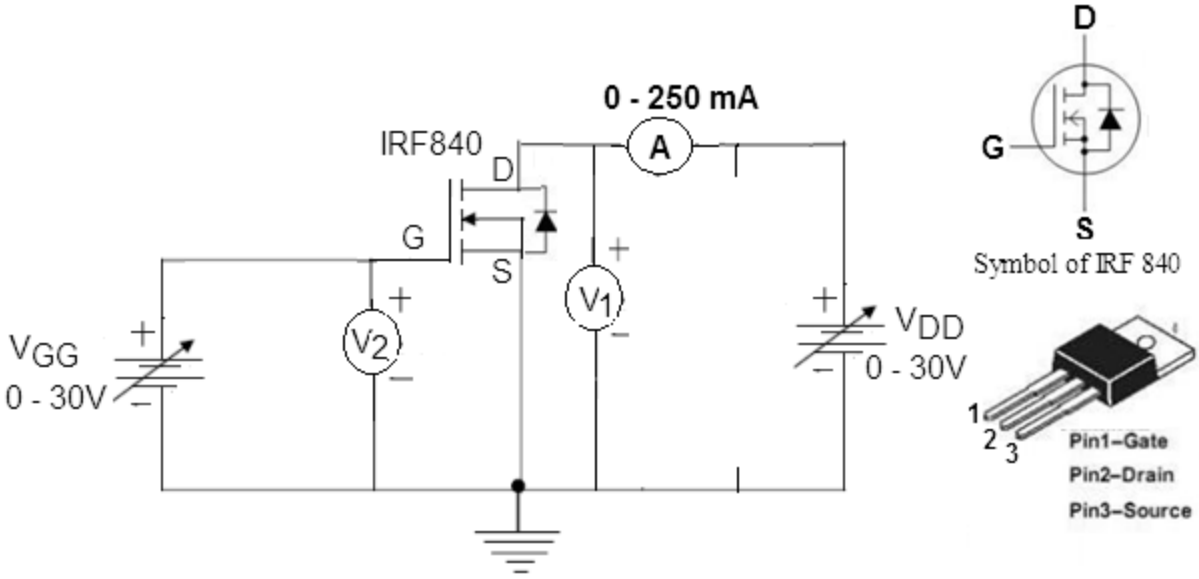
Drain and Transfer characteristics of a FET are studied.

CHARACTERISTICS OF MOSFET

AIM: To draw static characteristic of MOSFET and hence to determine the output resistance and Trans conductance.

APPARATUS REQUIRED: MOSFET – IRF840, 2.5KΩ/25W, Multimeters, patch chords.

CIRCUIT DIAGRAM:



Procedure:

Follow the below mentioned steps to obtain the **Drain Characteristics**

1. Set up the connections as indicated in the figure.
2. Keep both V_{GG} and V_{DD} at zero position.
3. By varying V_{GG} set V_{GS} to some value (slightly greater than the Threshold voltage determined from the transfer characteristics) Say 3.0V
4. Increase V_{DS} by varying V_{DD} gradually and note down the corresponding meter readings as shown in the table.
5. Repeat the steps 3 and 4 for V_{GS}=3.2V and V_{GS} = 3.4V
6. Plot the graph of I_D Vs V_{DS}

.. TABLE – Drain Characteristics

$V_{GS} = V_2$ = 3.0 (3.2V, 3.4V)

$V_{DS} = V_1$, V	0.2	0.4	0.6	0.8	1.0	1.5	2.0	3.0	5.0	10	12	15	18	20
I_D, mA														

Follow the below mentioned steps to obtain the **Drain Characteristics**

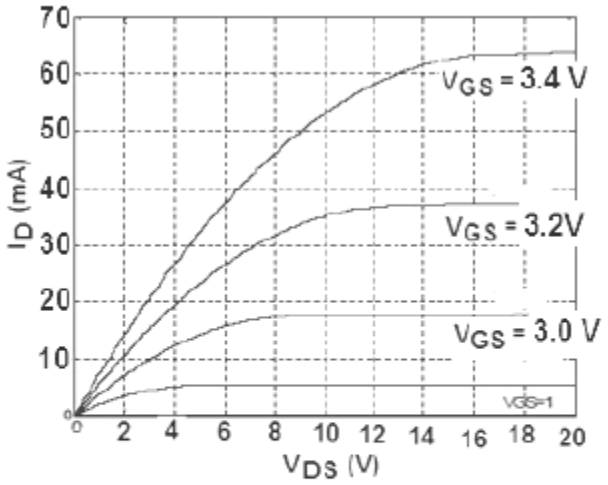
1. Set up the connections as indicated in the figure.
2. Keep both V_{GG} and V_{DD} at zero position.
3. Vary the V_{DD} and set V_{DS} = 5V.
4. Increase V_{GS} by varying V_{GG} gradually and note down the corresponding meter readings as shown in the table.
5. Note down the minimum value of V_{GS} for which drain current starts flowing and record V_{TH} =
6. Repeat for V_{DS} = 10V and 15V.
7. Plot the graph of I_D Vs V_{GS}

. TABLE – Transfer Characteristics

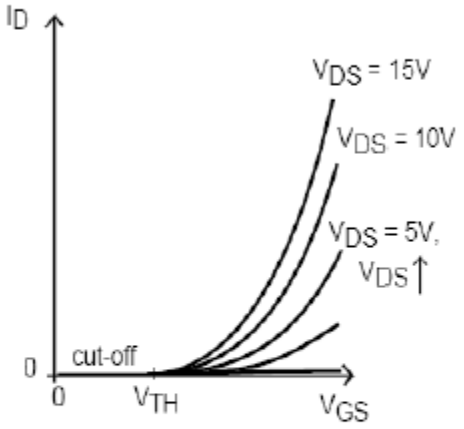
$V_{DS} = V_1$ = 5V (10V, 15V)

$V_{GS} = V_2$, V	1.0	2.0	2.8	2.9	3.0	3.1	3.2	3.3	3.4	3.5	3.8	4.0	4.2	4.5
I_D, mA														

Expected graphs:



Drain Characteristics

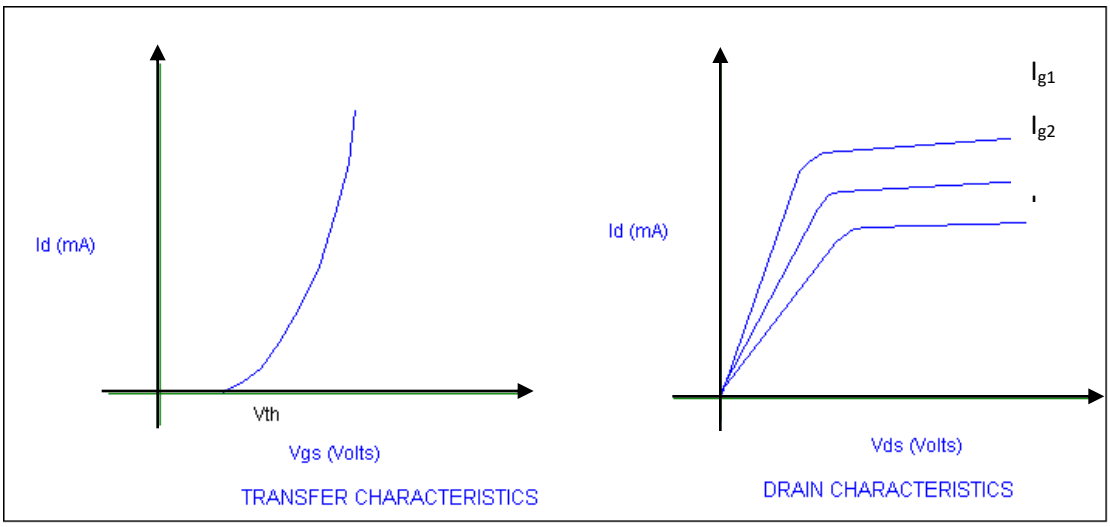


Transfer Characteristics

From the graphs determine

$g_m = (\Delta I_D/\Delta V_{GS})|_{VDS = Constant}$

$rd = (\Delta I_D/\Delta V_{DS})|_{VGS = Constant}$



PROCEDURE:

- Connect the circuit as shown in the fig 2.1 (a).
- Set V_{DS} = 10V by varying V1. Keep R1 slightly more than ¼ of the total value.
- Vary V_{GS} by varying V2 and note down I_{DS} for every 0.5V variation of V_{GS} till 5V of V_{GS}.
- Min V_{GS} voltage that is required for conduction is Threshold voltage" (V_{TH}).
- Repeat the above experiment for different values of V_{DS2} = 15V.

(b) Drain Characteristics:

- Rig up the circuit as shown in the fig 2.1(a).
- Adjust V_G by varying V_2 to $\mathbf{V_{TH}}$.
- Vary V_{DS} by varying V_1 in steps of 0.5v and note down I_{DS} (Till I_{DS} is constant).
- Repeat the above procedure for different values of V_{GS2} = $\mathbf{V_{TH}}$± 0.1 V.

O/P Resistance $R_D = \Delta V_{DS} / \Delta I_D$ **Trans conductance** $G_m = \Delta I_D / \Delta V_{DS}$

RESULT: The transfer characteristics & collector characteristics are obtained and their respective graphs are plotted and output resistance and Trans conductance are found.

11. UJT triggering circuit for Controller Rectifiers

AIM:

To Plot and study the characteristics of UJT & determine it's intrinsic standoff Ratio.

APPARATUS REQUIRED:

S. No.	Name	Range	Type	Qty
1	R.P.S	(0-30)V		2
2	Ammeter	(0–30)mA		1
3	Voltmeter	(0–30)V		1
		(0–10)V		1

COMPONENTS REQUIRED:

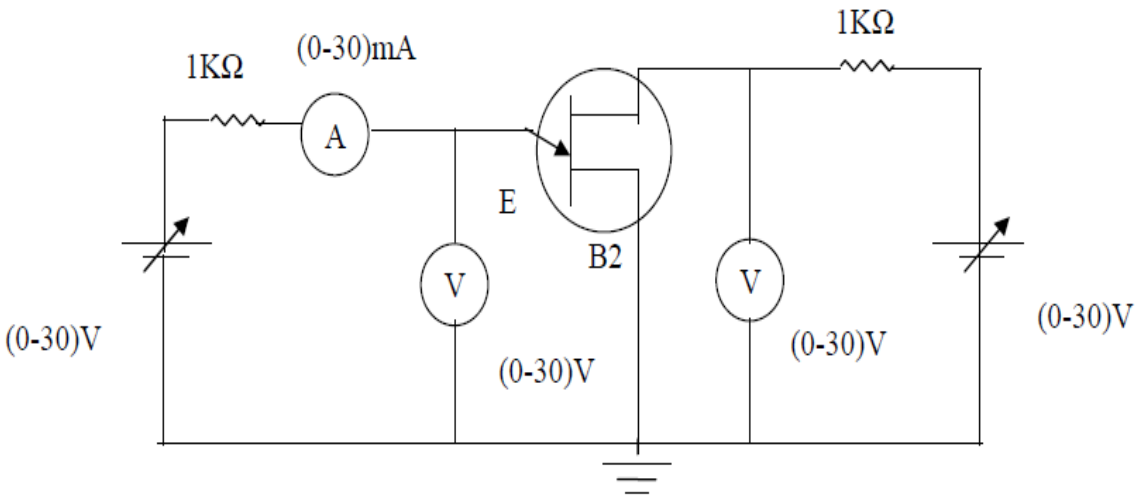
S. No.	Name	Range	Type	Qty
1	UJT	2N2646		1
2	Resistor	1KΩ		2
3	Bread Board			1

THEORY:

UJT(Double base diode) consists of a bar of lightly doped n-type silicon with a small piece of heavily doped P type material joined to one side. It has got three terminals. They are Emitter(E), Base1(B1),Base2(B2).Since the silicon bar is lightly doped, it has a high resistance & can be represented as two resistors, r_{B1} & r_{B2}. When V_{B1B2} = 0, a small increase in V_E forward biases the emitter junction. The resultant plot of V_E & I_E is simply the characteristics of forward biased diode with resistance. Increasing V_{EB1} reduces the emitter junction reverse bias. When $V_{EB1} = Vr_{B1}$ there is no forward or reverse bias. & I_E = 0. Increasing V_{EB1} beyond this point begins to forward bias the emitter junction. At the peak point, a small forward emitter current is flowing. This current is termed as peak current(I_P). Until this point UJT is said to be operating in cutoff region. When I_E increases beyond peak current the device enters the negative

resistance region. In which the resistance r_{B1} falls rapidly & V_E falls to the valley voltage.Vv. At this point I_E = Iv. A further increase of I_E causes the device to enter the saturation region.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{B1B2} = 0V, vary V_{EB1} , & note down the readings of I_E & V_{EB1}
3. Set V_{B1B2} = 10V , vary V_{EB1} , & note down the readings of I_E & V_{EB1}
4. Plot the graph : I_E Versus V_{EB1} for constant V_{B1B2}.
5. Find the intrinsic standoff ratio.

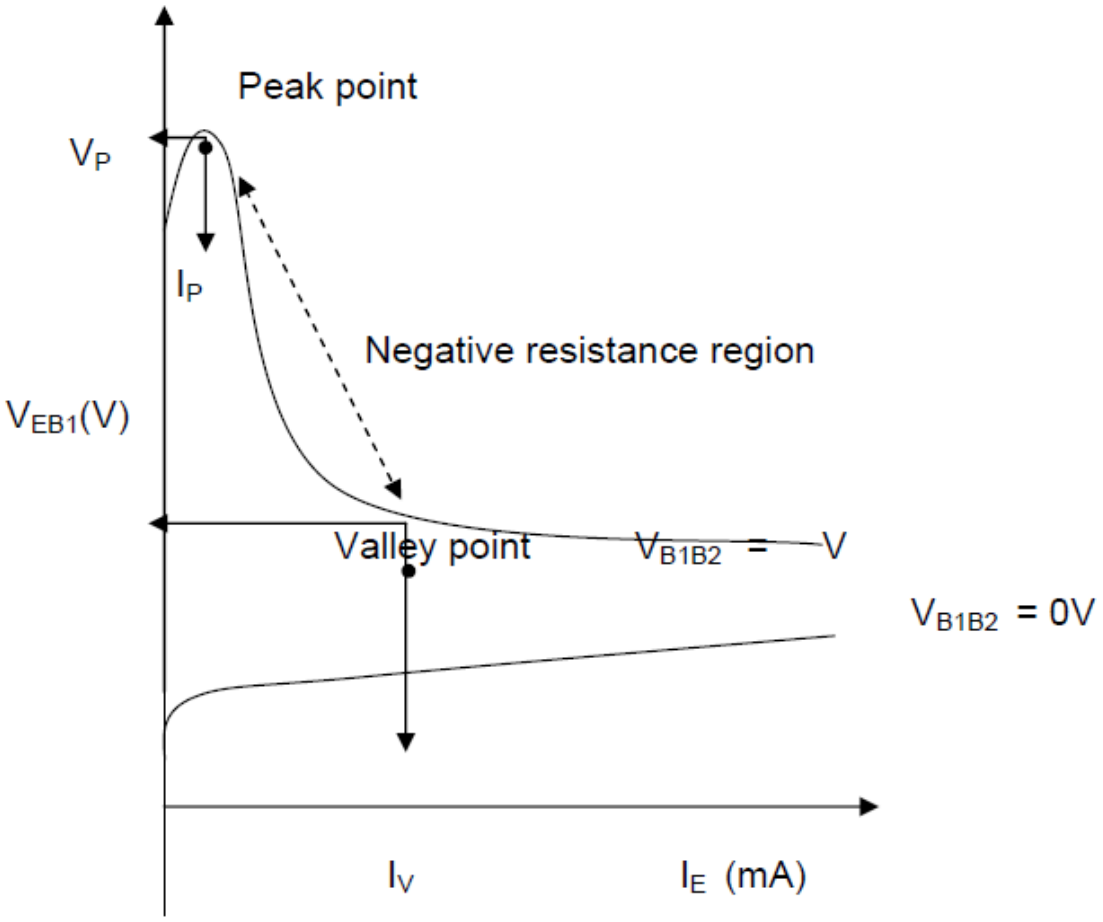
FORMULA FOR INTRINSIC STANDOFF RATIO:

$\eta = V_P - V_D / V_{B1B2}$., where V_D = 0.7V.

PROCEDURE:

1. Give the circuit connections as per the circuit diagram.
2. The dc input voltage is set to 20 V in RPS.
3. The output sweep waveform is measured using CRO.
4. The graph of output sweep waveform is plotted

MODEL GRAPH:



RESULT:

1. Thus the characteristics of given UJT was Plotted & its intrinsic standoff Ratio = ----.

12. Design and simulation of Regulated power supply

AIM:

To simulate and verify the function of regulated power supply.

COMPONENTS REQUIRED:

S.NO	COMPONENT	SPECIFICATION	QUANTITY
	transformer	12-0-12 1 A	1
	Diode	in4007-4	4
	Capacitor	1500uf 25v-1,	1
	Capacitor	0.1uf	2
	IC regulator	LM7805 for 5v	1

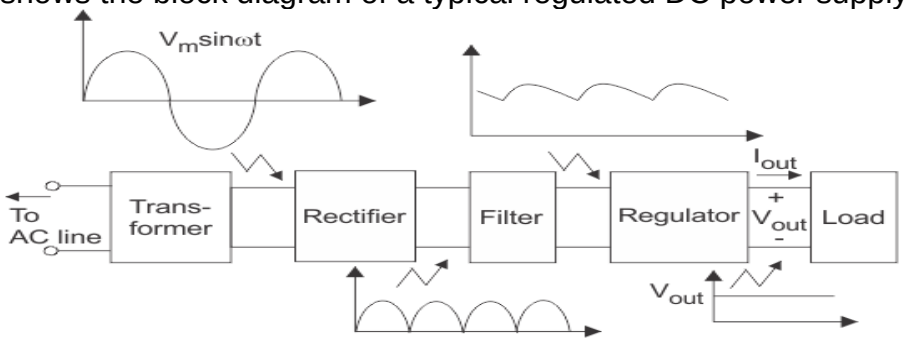
THEORY:

What is a Regulated Power Supply?

A **regulated power supply** converts unregulated AC (Alternating Current) to a constant DC (Direct Current). A regulated power supply is used to ensure that the output remains constant even if the input changes.

A regulated DC power supply is also known as a linear power supply, it is an embedded circuit and consists of various blocks.

The regulated power supply will accept an AC input and give a constant DC output. The figure below shows the block diagram of a typical regulated DC power supply.



Components of typical linear power supply

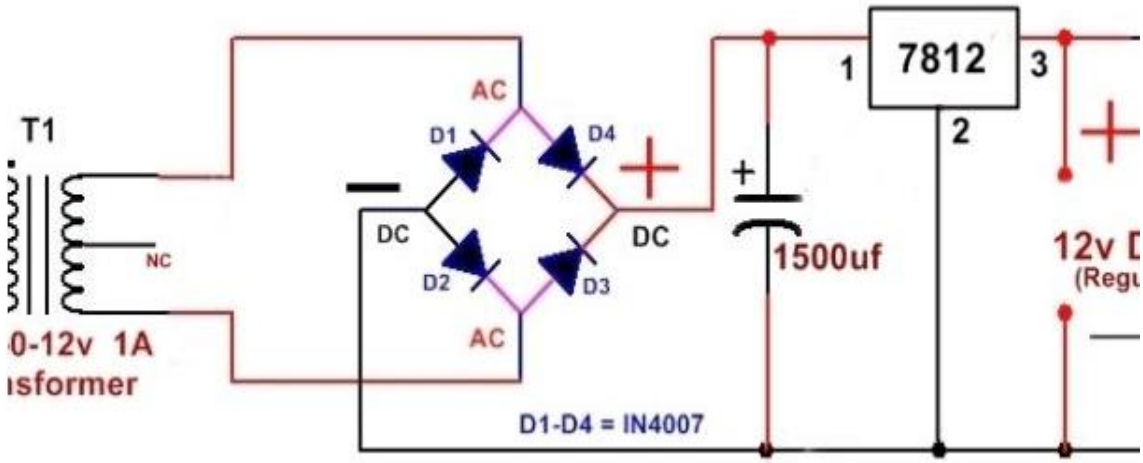
1. The first stage is in AC to DC is to make down the voltage as required level using step down transformer

2. Second stage is the Rectifing the signal , Rectifiers are used to rectifying the signal. Rectifying means convert the ac signal to dc as possible.

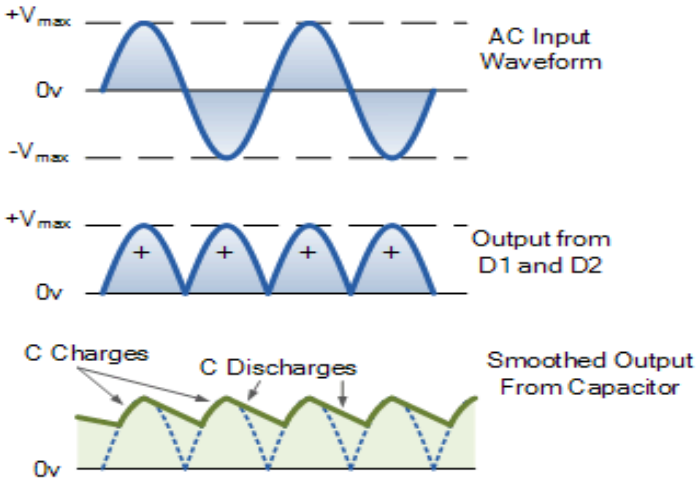
3. Third stage is Filter the signal . After rectifyng the signal it consists ripple noise in dc signal that is not perfectly suitable for operate the circuit. Capacitor is used to filter the signal.

4. Fourth stage is the Regulation, Regulation make the more stable of any signal to give the circuit to constant supply. Regulator ic or Zener diode is used to make the constant signal.

CIRCUIT DIAGRAM:



EXPECTED INPUT AND OUTPUT WAVEFORMS:



OUTPUT WAVEFORM

SIMULATION RESULT: