ATRIA INSTITUTE OF TECHNOLOGY

(Affiliated To Visvesvaraya Technological University, Belgaum)

Anandanagar, Bangalore-24

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

ANALOG CIRCUITS LAB MANUAL

FOURTH SEMESTER ELECTRONICS AND COMMUNICATION

SUBJECT CODE: 18ECL48

2019-20

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ANALOG CIRCUITS LAB MANUAL

The Computer Networks Laboratory Manual pertaining IV semester ECE has been prepared as per VTU syllabus and all the experiments are designed, tested and verified according to the experiment list.

This manual typically contains practical/lab sessions related to know the function and design of various analog circuits like amplifiers, oscillators, filters etc. Simulation of circuits using multisim helps the students to relate this to the subject for better understanding. Students are advised to thoroughly go through this manual as it provides them practical insights.

Good Luck for your Enjoyable Laboratory Sessions

DEPARTMENT VISION & MISSION

Vision

"Imparting quality technical education through interdisciplinary research & innovation towards moulding the young talent with professional competence and ethical values for developing inclusive and sustainable technology in the area of Electronics and Communication Engineering".

Mission

Create conducive environment for the holistic development of students and staff members.

- Provide quality technical education to produce industry ready engineers with an entrepreneurial and research outlook.
- Establish centers of excellence in collaboration with industries/universities for exposing the students to latest technologies.
- Nurture the students to actively participate in solving the societal problems and uphold ethics and morality.
- To train the students to meet global challenges in interdisciplinary fields by inculcating a quest for modern technologies in the emerging areas.

ATRIA INSTITUTE OF TECHNOLOGY
1st Main, AG's Colony, Anandanagar, Bangalore- 560024
Department of Electronics and Communication

ANALOG CIRCUITS LABORATORY

Sub code: 18ECL48 **Class: IV SEM EC**

Course Learning Objectives: This laboratory course enables students to

- Understand the circuit configurations and connectivity of BJT and FET Amplifiers and Study of frequency response
- Design and test of analog circuits using OPAMPs
- Understand the feedback configurations of transistor and OPAMP circuits
- Use of circuit simulation for the analysis of electronic circuits.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Design analog circuits using BJT/FETs and evaluate their performance characteristics.
- Design analog circuits using OPAMPs for different applications
- Simulate and analyze analog circuits that usesICs for different electronic applications.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

PART A : Hardware Experiments

1. Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response.

2. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.

3. Design and set-up BJT/FET i) Colpitts Oscillator, and ii) Crystal Oscillator

4. Design active second order Butterworth low pass and high pass filters.

5. Design Adder, Integrator and Differentiator circuits using Op-Amp

6. Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.

7. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.

8. Design Monostable and AstableMultivibrator using 555 Timer.

PART-B : Simulation using EDA software (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab orany other equivalent tool can be used)

1. RC Phase shift oscillator and Hartley oscillator
2. Narrow Band-pass Filter and Narrow band-reject filter
3. Precision Half and full wave rectifier
4. Monostable and AstableMultivibrator using 555 Timer.

EXPERIMENT 1

COMMON EMITTER AMPLIFIER

Aim: Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.

Components and equipments required: Transistor – SL100, Resistors - 470 Ω, 1KΩ, 10KΩ - 2nos, and 33KΩ, Capacitors 100µf, 0.22µf and 0.47µf, Power Supply, 10Hz – 3MHz Signal generator, CRO, Connecting wires and Bread board/Spring board with spring terminals.

Design:

Transistor: **SL100**

Let VCC = 12V; IC = 4.5 mA; VE = 1.2V; VCE = 6V;

hFE = 100.

Given VE = 1.2V. Therefore RE = VE / IE VE / IC =266.67Ω; **RE =270Ω**

Writing KVL for the Collector loop we get, VCC = ICRC + VCE + VE

 RC = (VCC – VCE – VE) / IC = (12-6-1.2)V/4mA=1.06KΩ; **RC = 1 KΩ**

hFE RE = 10R2

Assume **R2=2.7KΩ,**

VB = (Vcc x R2) / (R1 + R2)

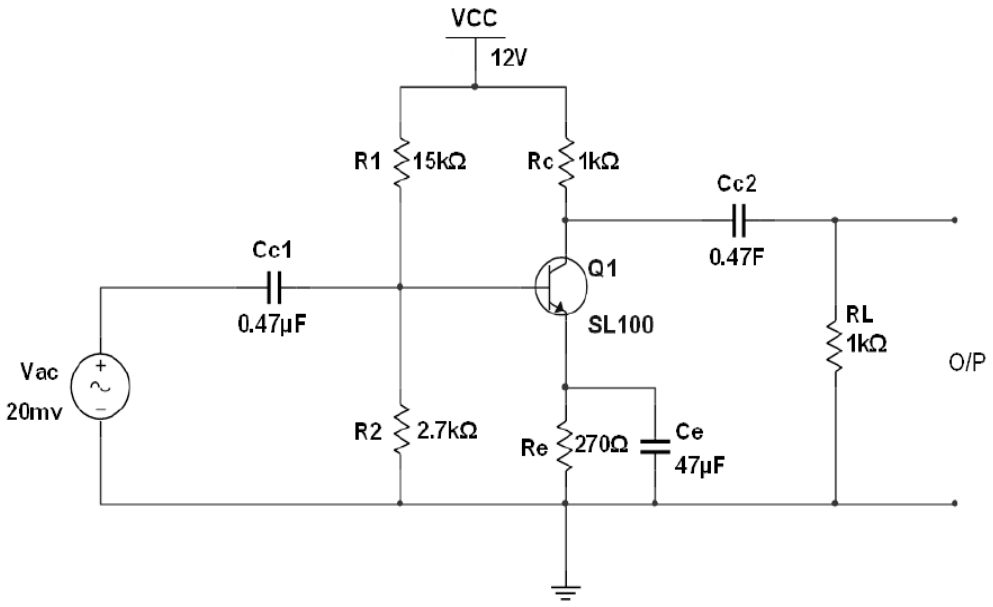
Hence R1 = 14.14 KΩ ; **R1 = 15 KΩ**

Use **CC1 = 0.47µF**

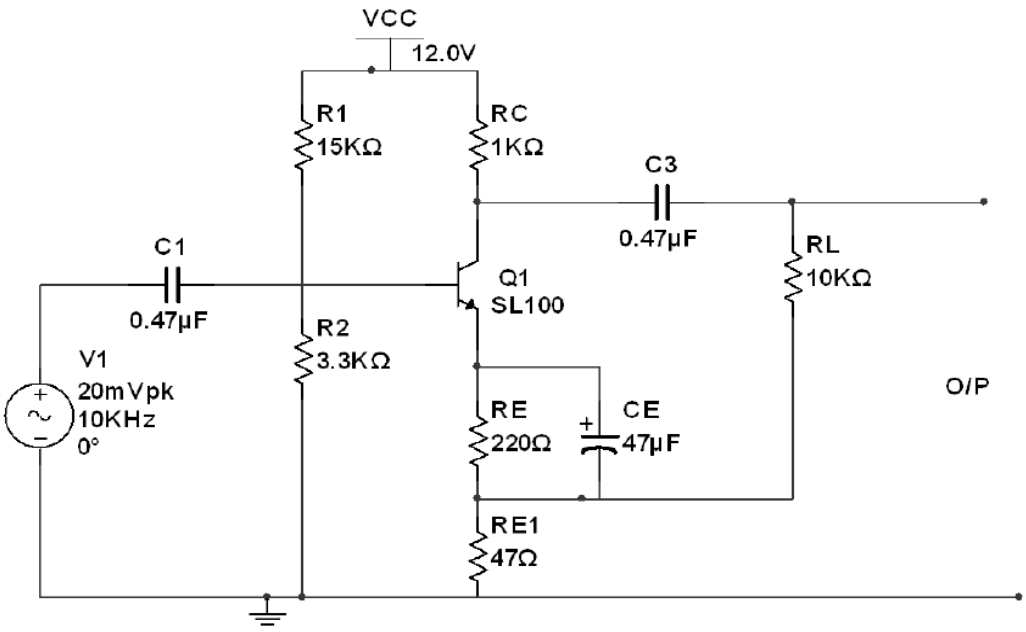
Use **CC2 = 0.47µF**

Use **CE =47µF**

Circuit Diagram of amplifier without feedback



Circuit Diagram of amplifier with feedback. (introduce a resistor in the emitter circuit)



Procedure:

Follow the same procedure for both circuits

1. After making the connections, switch on the D.C. power supply and check the D.C. conditions without any input signal and record in table below:
2. Select sine wave input and set the input signal frequency ≥10f1 (Say = 10 KHz. This will be a convenient 'Mid – frequency').
3. Observe the input wave form and output wave form on a dual channel CRO.
4. Adjust the input amplitude such that the output waveform is just undistorted (or in the verge of becoming distorted). Measure the amplitude of the Input Signal now. **This amplitude is the Maximum Signal Handling Capacity of your amplifier.**
5. Decrease the input voltage to a convenient value such that the output is undistorted. **Say 20mV**. Measure the corresponding o/p voltage. Calculate mid-band gain, **AM = Vo (p-p) / Vin (p-p).**
6. Keeping the input voltage constant, go on reducing the frequency until the output voltage reduces to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Lower Cut-off frequency (*f1*).
7. Keeping the input voltage constant, go on increasing the frequency until the output voltage decreases to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Upper Cut-off frequency (*f2*).
8. Thus you have pre-determined *f1* and *f2*. Find the amplifier band width,
BW = *f2 – f1*
9. Determine Gain Bandwidth product (GBW product) which is a Figure of Merit of your amplifier as GBW = AM x BW.
10. Now repeat the experiment by recording values of output voltage versus frequency keeping the input

voltage at a constant value convenient to you. You should take at least 5 readings below *f1* and 5 readings above *f1*, at least 5 readings in the mid band, at least 5 readings below *f2* and 5 readings above *f2*.

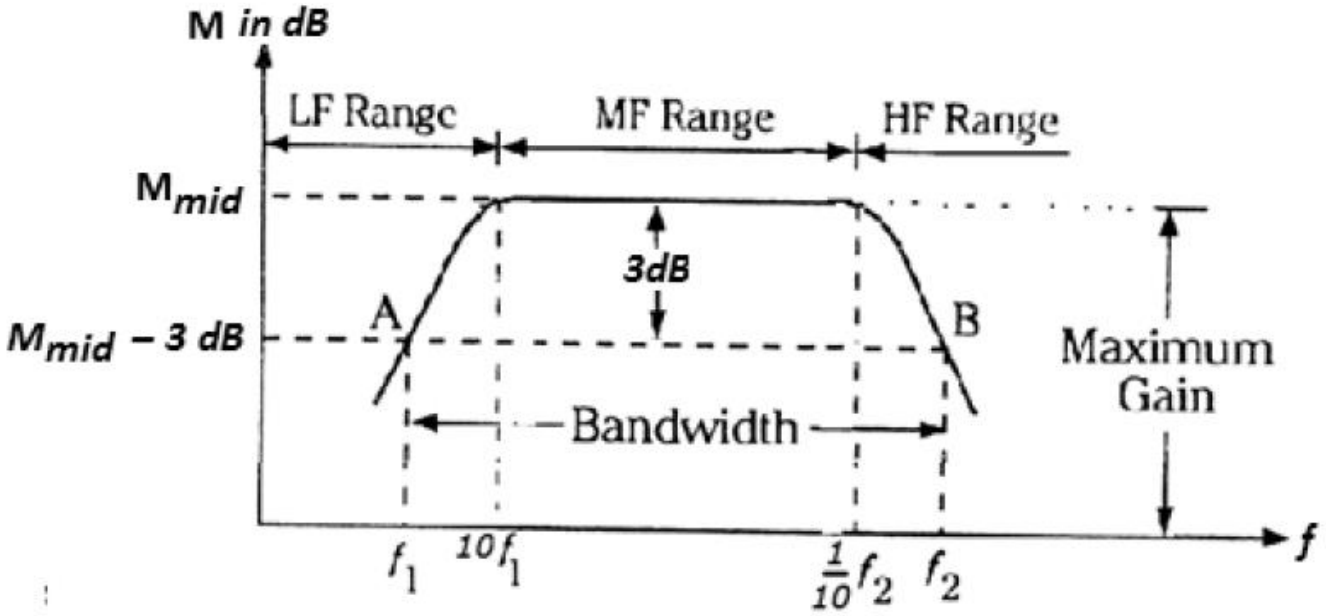
11. Plot graphs of AV versus Frequency, *f* and /or M, dB versus Frequency, *f* on a ***semi log graph paper***. From the graph determine: Mid –band - gain, Lower and Upper Cut-off frequencies and Band width. Compute the GBW product and verify with answer obtained earlier.

Parameter	V_{RC}	V_{CE}	V_E	I_{CQ}	V_{BE}
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V
Practical					

Observation: Use the tabular column separately for each circuit
Vin (P-P) = …….. V
AV= VO (P-P)/Vin (P-P)
M = 20log (AV), dB

Frequency In Hz	100	200	300	350	400	500	600	700	800	1K	2K	3K	5K	8K
V_O(P-P) in Volts														
A_V														
M, dB, (A_V in dB)														
Frequency In Hz	10K	20K	30K	50K	100K	200K	300K	400K	500K	600K	700K	800K	900K	1M
V_O(P-P) in Volts														
A_V														
M, dB, (A_V in dB)														

Expected graph



Result:

Thus the frequency response analysis of CE amplifier with and without feedback are done.

EXPERIMENT 2

2.JFET/MOSFET AMPLIFIER

Aim: Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.

Components and equipments required: JFET – BFW10, Resistors - 180 Ω, 1KΩ, 10KΩ and 1MΩ, Capacitors 47µf, 0.1µf and 0.047µf, Power Supply, 10Hz – 3MHz Signal generator, CRO, Connecting wires and Bread board/Spring board with spring terminals.

Design:
For BFW10 Junction FET specifications are as below:
VDS max = 30 V, VGS off = -8 V, IDSS min = 8mA, IDSS max = 20mA
Choose IDSS (Min + Max)/2 = (8 + 20)/2= 14 mA,
VP = Max/2 = - 4 V and *g*m = 3.5 to 6.5 m-mhos
Quiscent-Conditions: IDQ = IDSS/2 = 7mA,
Let IDQ = 5 mA. VDD=12V, VDSQ=VDD / 2=6V
Using these values, we get

$$R_s = \frac{|V_p|}{I_{DQ}}\left(1 - \sqrt{\frac{I_{DQ}}{I_{DSS}}}\right) = 0.3219K\Omega$$

let Rs = 330Ω

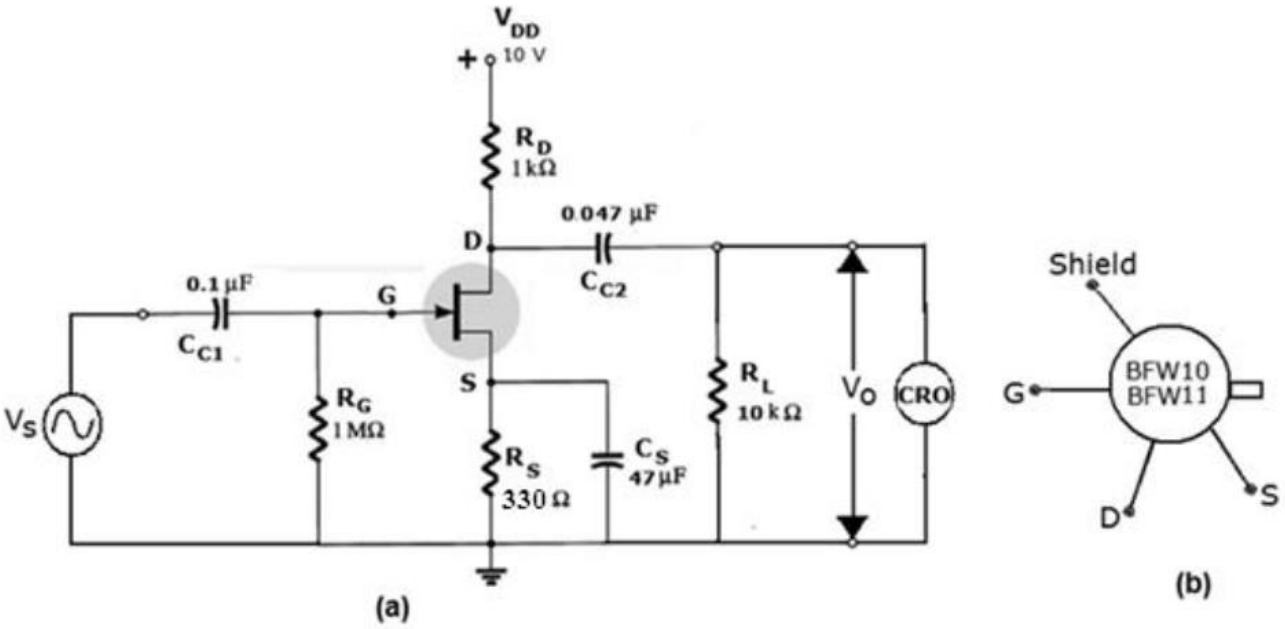
With this choice of Rs, VS = RSIDQ = 1.65 V

$$R_D = \frac{V_{DD} - V_{DQ} - V_S}{I_{DQ}} = 0.87K\Omega$$

Let RD=1.0 KΩ

RG may be chosen arbitrarily but should be large enough such that overall input impedance is not affected much. Let RG=1.0 MΩ
CC1 = 1/2л*f1*Ri will be very small because of large Ri and chosen to be much larger so that it does not decide *f1*. Thus CC1=0.1µF
Let RL=10KΩ and *f1*=300Hz
Typical value of output admittance for BFW10, *gd* =85µ Mhos
That is, *rd* =1/ *gd* = 12KΩ. Therefore RD||*rd* ≈RD=1KΩ
Now, CC2=1/2л*f1* (RD+RL) =0.0482µF Thus select CC2=0.047µF
Choosing XCs=RS/10 = 18Ω at *f1*/2=150Hz, we get CS=58.9µF let CS=47µF or CS= 100 µF

Circuit Diagram:



Procedure:

1. Switch on the D.C. power supply and check the D.C. conditions without any input signal and record in table below:

Parameter	V_{DD}	V_{RD}	V_{DS}	V_S	I_{DQ}	V_{GS}
Assumed	12V	4.35V	6 V	1.65V	5mA	-1.65V
Practical						

2. Select
sine wave
input and set the input signal frequency ≥10f1 (Say = 10 KHz. This will be a convenient 'Mid – frequency').
3. Observe the input wave form and output wave form on a dual channel CRO.
4. Adjust the input amplitude such that the output waveform is just undistorted (or in the verge of becoming distorted). Measure the amplitude of the Input Signal now. **This amplitude is the Maximum Signal Handling Capacity of your amplifier.**
5. Decrease the input voltage to a convenient value such that the output is undistorted. **Say 100mV**. Measure the corresponding o/p voltage. Calculate mid-band gain, **AM = Vo (p-p) / Vin (p-p).**
6. Keeping the input voltage constant, go on reducing the frequency until the output voltage reduces to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Lower Cut-off frequency (*f1*).
7. Keeping the input voltage constant, go on increasing the frequency until the output voltage decreases to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Upper Cut-off

frequency (*f2*).
8. Thus you have pre-determined *f1* and *f2*. Find the amplifier band width, BW = *f2 – f1*
9. Determine Gain Bandwidth product (GBW product) which is a Figure of Merit of your amplifier as GBW = AM x BW.
10. Now repeat the experiment by recording values of output voltage versus frequency keeping the input voltage at a constant value convenient to you. You should take at least five readings below *f1* and 5 readings above *f1*, at least 5 readings in the mid band, at least 5 readings below *f2* and 5 readings above *f2*.
11. Plot graphs of AV versus Frequency, *f* and /or M, dB versus Frequency, *f* on a ***semi-log graph paper***. From the graph determine: Mid –band - gain, Lower and Upper Cut-off frequencies and Band width. Compute the GBW product and verify with answer obtained earlier.
Vin (P-P) = ……..Volts (Constant)

Frequency In Hz	100	200	300	350	400	450	500	600	800	1K
V_O(P-P) in Volts										
A_V										
M, dB (A_V in dB)										

Frequency In Hz	2K	3K	5K	8K	10K	20K	30K	50K	100K	200K
V_O(P-P) in Volts										
A_V										
M, dB (A_V in dB)										

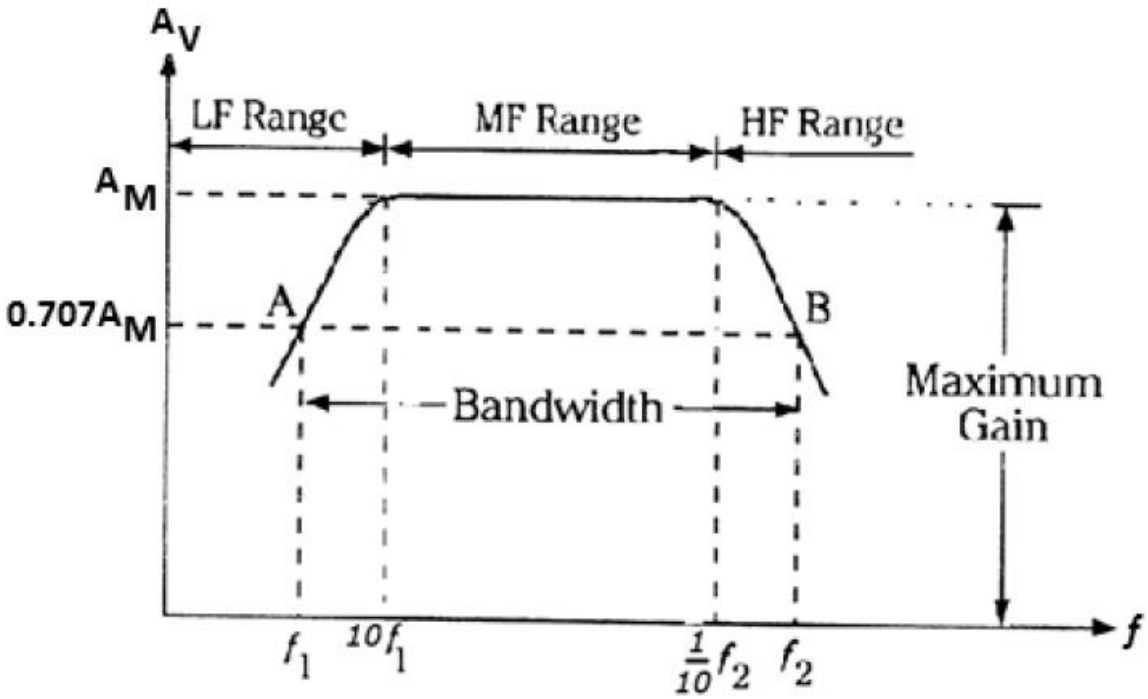
requency In Hz	300K	500K	800K	1M	1.5M	1.8M	2M	2.5M	2.8M	3M
V_O(P-P) in Volts										
A_V										
M, dB (A_V in dB)										

A_V= V_O (P-P)/V_{in} (P-P) (It is a ratio of two voltages. No units); M = 20*log* (A_V), dB

Result:

Thus the frequency response analysis of JFET and MOSFTET amplifier are analysed.

Expected Graphs:



Plot of Voltage Gain AV versus frequency

EXPERIMENT 3

3(a).COLPITTS OSCILLATOR

Aim: Design and set-up the following tuned oscillator circuit using BJT, and determine the frequency of oscillation.
Colpitts Oscillator

LC oscillators are generally used as RF oscillators since they generally used to create high frequency oscillations. In Colpitts oscillator an LC tank circuit is used for selection of frequency of oscillation. A voltage divider biased common emitter amplifier is used as amplifier. The amplifier and tank circuit together provides a phase shift of 360 degrees to satisfy Barkhausen criterion.

Components and equipments required: Transistor SL 100, Resistors 470Ω, 1KΩ 10KΩ and 33 KΩ; Capacitors 0.1μf - 3nos, Discrete inductances 100 μH – 2 nos, Capacitor 470 pF – 2nos, Power supply, CRO, Connecting wires etc.

Design:

BJT- Amplifier design is same as given in Common Emitter Amplifier**.**

Tank Circuit Design: $f = \frac{1}{2\pi\sqrt{LC_{eq}}}$ Where $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$

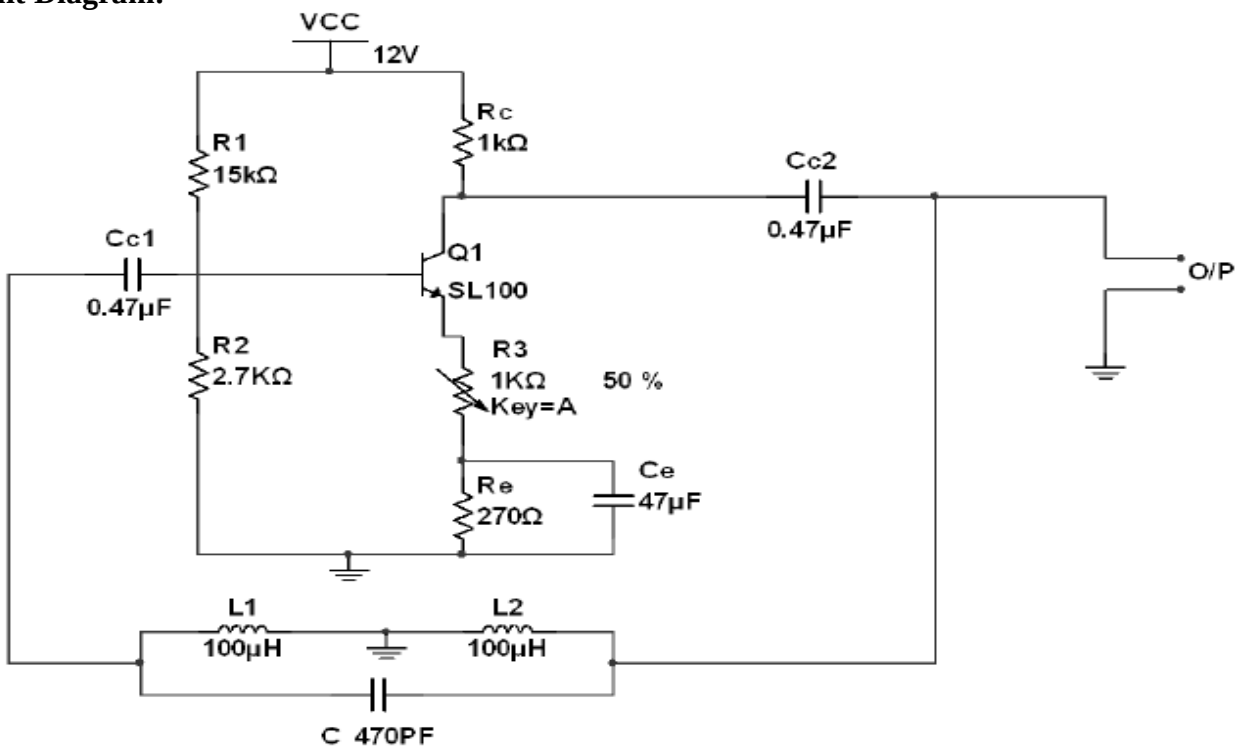
Given Oscillation frequency f=1 MHz

Assume C_1=C_2 = 470 pF ∴ C_{eq}= 235 pF =$2.35 * 10^{-10}$F

Then, $L = \frac{1}{4\pi^2 (f^2) C} = 119\ \mu H$

Use L = 100 μH, For this value of L, f = 1.04 MHz

Circuit Diagram:



Procedure:

1. Switch on the Power Supply and check the D.C conditions by removing the coupling capacitor CC1 or CC2.
2. Connect the coupling capacitors and obtain an output waveform on the CRO. If the o/p is distorted adjust 1- KΩ Potentiometer (R3) to get perfect SINE wave.
3. Measure the period of oscillation and calculate the frequency of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected.

Observation:

Parameter	V_{RC}	V_{CE}	V_E	$I_{CQ} = V_{RC} / R_C$	V_{BE}	V_B
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V
Practical						

Result: The frequency of oscillation is **…..**

3.(b)CRYSTAL OSCILLATOR

Aim: Design and set-up the crystal oscillator and determine the frequency of oscillation.

Components and equipments required:
Transistor SL 100, Crystal – 2MHz, Resistors 470Ω, 1KΩ 10KΩ and 33 KΩ; Capacitors 0.1μf - 2nos, Power supply, CRO, Connecting wires etc.

Theory:
Crystal oscillators are used in order to get stable sinusoidal signals despite of variations in temperature, humidity, transistor and circuit parameters. A piezo electric crystal is used in this oscillator as resonant tank circuit. Crystal works under the principal of piezo-electric effect. i.e., when an AC signal applied across the crystal, it vibrates at the frequency of the applied voltage. Conversely if the crystal is forced to vibrate it will generate an AC signal. Commonly used crystals are Quartz, Rochelle salt etc.

Design:
Let VCC = 12V;
ICQ = 4mA;
VE = (1/10) VCC to (1/5) VCC;
VCE=Vcc/2 = 6V;
hFE = 100.

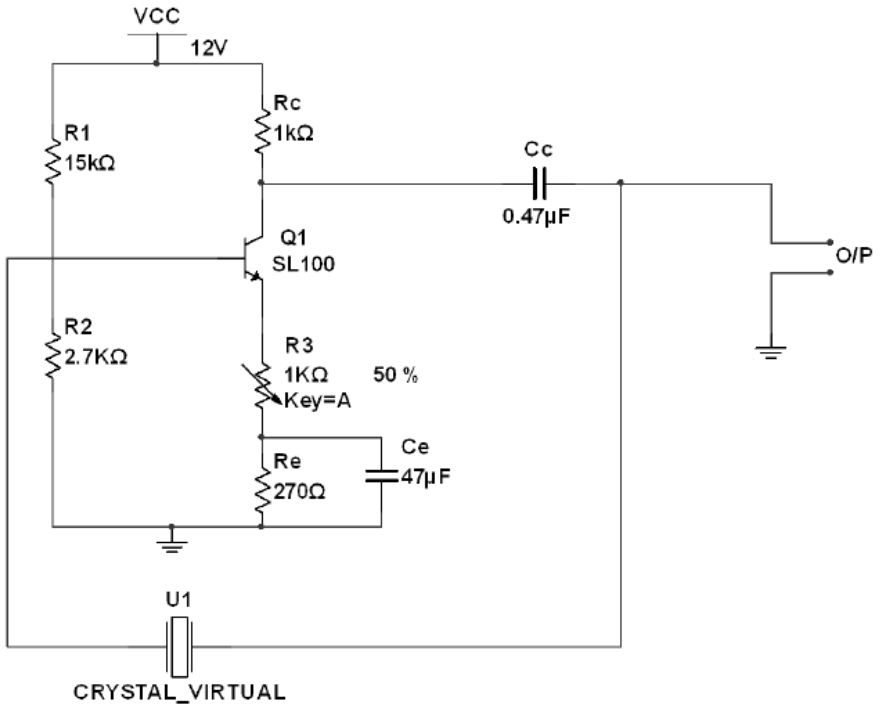
To find RE: Let us choose **VE = 2 V**
RE = VE / IE= VE / IC =2 V/ 4 mA =500 Ω; let **RE =470Ω**
VCC = ICRC + VCEQ + VEQ
RC = (VCC – VCEQ– VEQ) / ICQ = 4.0 V/ 4mA =1.0K **Ω; RC= 1K Ω**

Assume R2=10kΩ.
VB = VE + VBE = 2 + 0.6 = 2.6V
I2 = Current through R2= VB /R2 = 0.26mA or 260μA

The base current IB = IC / hFE= 4mA / 100= 0.04mA= 40μA
(hFE = βDC = 100, a working value; It varies from 50 to 280 for SL 100)
I1 = Current through R1 = IB+I2 = 300 μA
VR1=VCC– VB=12 – 2.6 =9.4V
R1 =VR1/ I1= 9.4V/300 μA =9400/300 KΩ =31.33KΩ **R1 = 33K Ω**
CE = CC =0.1μF (Arbitrary, any value which gives a reactance < 10 Ω at Crystal frequency may be used. reactance of a Capacitor XC = (1/2πfC);

For C = 0.1 μF, XC = 0.8Ω at 2 MHz)

Circuit Diagram:



Procedure:

1. Switch on the Power Supply and before inserting the crystal check the D.C conditions by removing the coupling capacitor CC1 or CC2.
2. Insert the crystal and the coupling capacitors and obtain the output waveform on the CRO. If the o/p is distorted vary 1- KΩ Potentiometer (R3)to get perfect SINE wave.
3. Measure the period of oscillation and calculate the frequency of oscillation.
4. Compare with frequency marked on the crystal.

Observation:

Parameter	V_{RC}	V_{CE}	V_E	$I_{CQ} = V_{RC} / R_C$	V_{BE}	V_B
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V
Practical						

Result:

Thus the given crystal oscillator designed frequency has been verified.

EXPERIMENT-4

Design active second order Butterworth low pass and high pass filters.

Second Order Active Low Pass Filter

Aim:-To design active second order Butterworth low pass for cutoff frequency 5KHz

Components Required: Op-Amp µA-741, Resistors, Capacitor, Signal Generator, CRO, Fixed Power supply +12V,0,-12V.

Circuit Diagram:

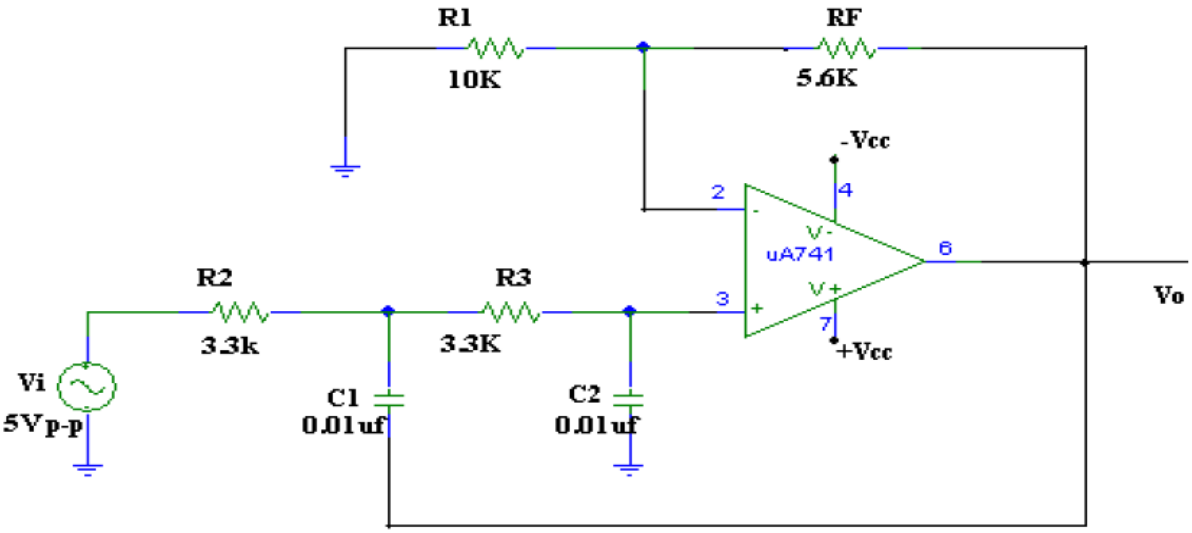


Figure1. Second order active low pass filter.

Design:

Let A_f =1.568 & fc=5KHz

$A_f = [1 + (R_f/R1)]$

$1.568-1 = R_f / R1$

R_f =5.6 KΩ, When R1=10 KΩ

$fc = 1 / 2\pi Rc$ assume c=0.01µF

$R=R2=R3=1 / (2\pi X\ 5x10^3\ X\ 0.01x10^{-6}) = 3.3K\Omega$

(We can also Choose R_f = (1 kΩ resistor + 10 kΩ potentiometer) for better gain)

Procedure:-

1. Ckt connections are made as shown in the fig.
2. Input voltage is kept constant at 2V p-p
3. The input frequency is varied from 100Hz to 30 KHz
4. At each step corresponding output is measured.
5. The gain in dB is calculated by using the formula AF=20 log (V_o/V_i)

6. The graph of gain v/s frequency is plotted on the graph sheet.

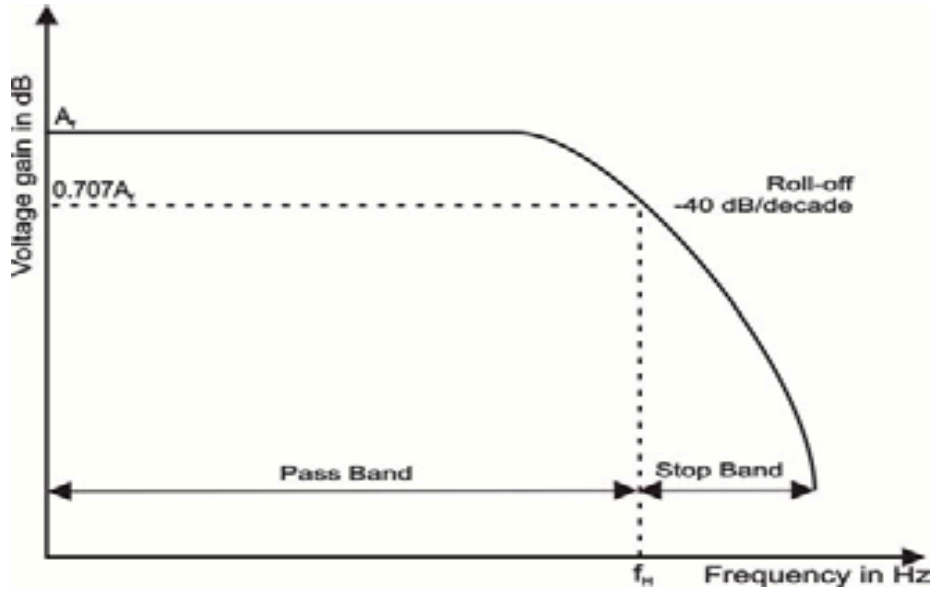
7. The higher cut-off frequency, roll-off rate are calculated and compared with Theoretical values.

To find the Roll-off factor for LPF:- Keep the input signal amplitude constant, adjust the input frequency at $10f_c$,note the output signal amplitude. The difference in the gain of the filter at f_c and $10f_c$ gives the roll-off factor**.**

Tabular Column:

Frequency f	Vo volts	G = 20 log (Vo/Vi) db		Frequency f	Vo volts	G = 20 log (Vo/Vi) db
100 Hz				2 kHz		
200 Hz				3 kHz		
300 Hz				4 kHz		
400 Hz				5 kHz		
500 Hz				6 kHz		
600 Hz				7 kHz		
700 Hz				8 kHz		
800 Hz				9 kHz		
900 Hz				10 kHz		
1 kHz				20khz		

Graph: Frequency Response for Low Pass Filter



Result: -

Cut-off frequency = _____ ,

Roll-off factor = _____

Second Order Active High Pass Filter

Aim: To design an active second order high pass filter for cutoff frequency 5 KHz

Components Required: Op-Amp µA-741, Resistors, Capacitor, Signal Generator, CRO, Fixed Power supply +12V,0,-12V.

Circuit Diagram:

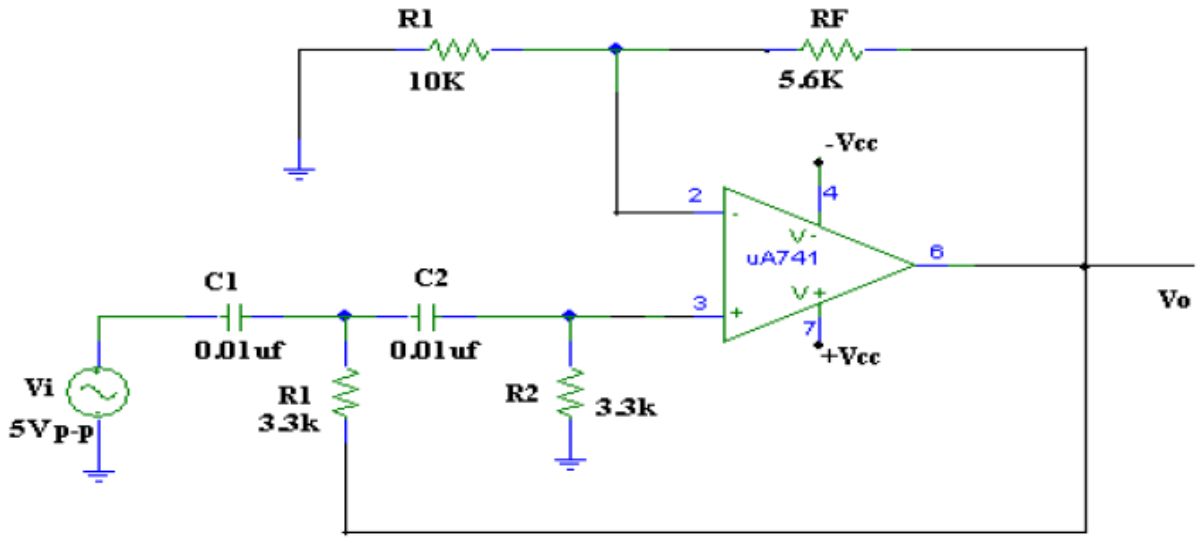


Figure2. Second order active High pass filter.

Design:

Let A_f =1.568 & fc=5KHz

$A_f = [1 + (R_f/R1)]$

$1.568-1 = R_f / R1$

R_f =5.6 KΩ , When R1=10 KΩ

fc = 1 / 2πRc assume c=0.01µF

$R=R2=R3=1 / (2\pi X\ 5x10^{3}\ X\ 0.01x10^{-6}) = 3.3K\Omega$

Procedure:

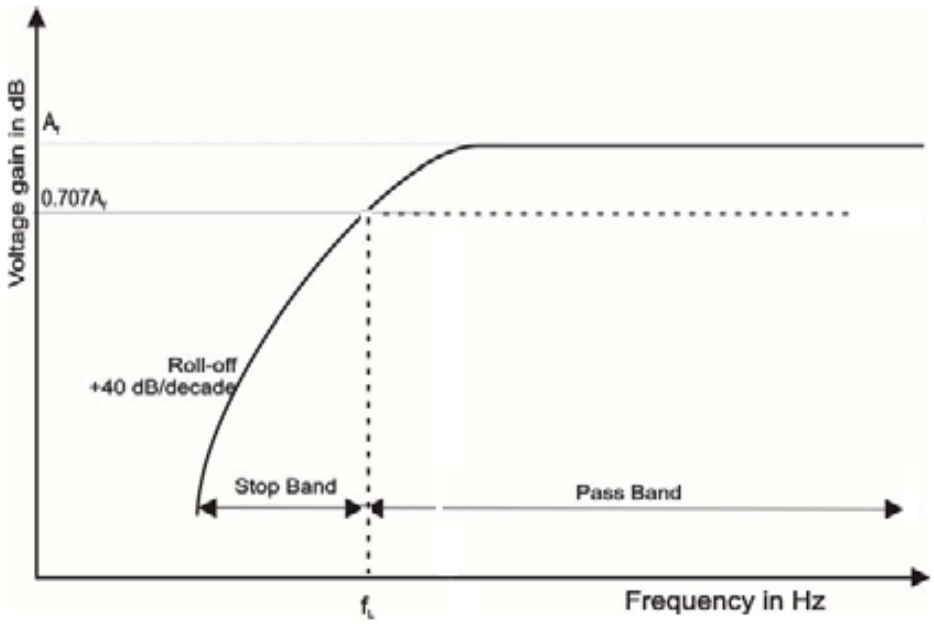
1. Ckt connections are made as shown in the fig.
2. Input voltage is kept constant at (2V P-P)
3. The input frequency is varied from 100Hz to 50 KHz
4. At each step corresponding output readings are measured.
5. The gain in dB is calculated by using the formula Af=20 log vo/vi
6. The graph of gain v/s frequency is plotted on the graph sheet.
7. The higher cut-off frequency, roll-off rate are calculated and compared with theoretical values.

To find the Roll-off factor for HPF:- Keep the input signal amplitude constant, adjust the input frequency at 0.1fc,note the output signal amplitude. The difference in the gain of the filter at fc and 0.1fc gives the roll-off factor

Tabular Column:

Frequency Hz	Vo volts	G = 20 log (Vo/Vi) db		Frequency f	Vo volts	G = 20 log (Vo/Vi)
100 Hz				2 kHz		
200 Hz				3 kHz		
300 Hz				4 kHz		
400 Hz				5 kHz		
500 Hz				6 kHz		
600 Hz				7 kHz		
700 Hz				8 kHz		
800 Hz				9 kHz		
900 Hz				10 kHz		
1 kHz				20kHz		

Graph: Frequency Response for High Pass Filter



Result: -

Cut-off frequency = _____

Roll-off factor = _____

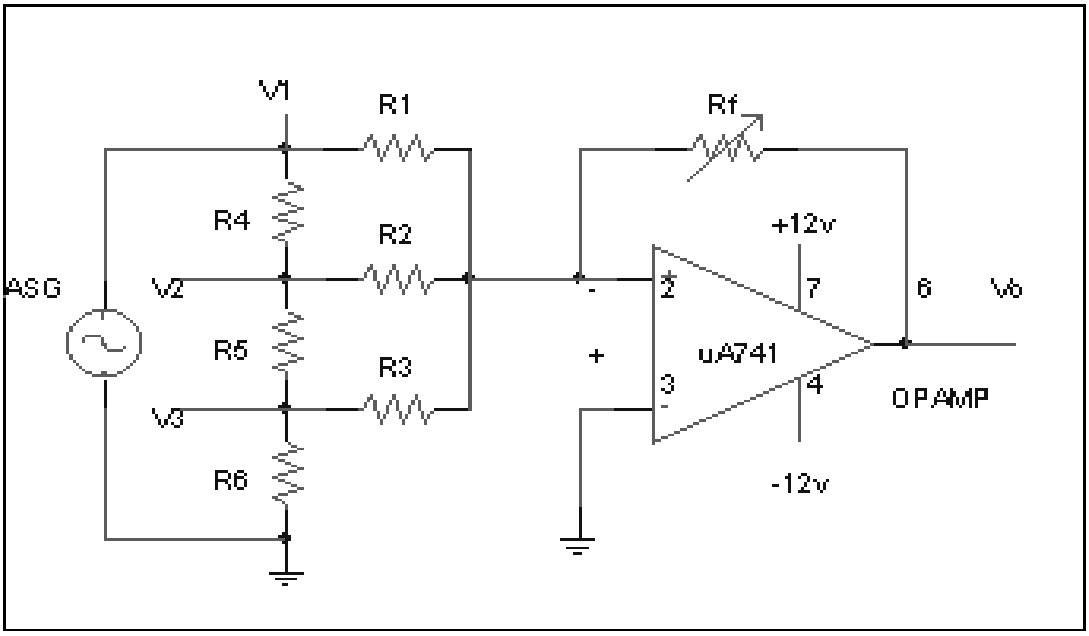
EXPERIMENT-5

Aim: To design operational amplifier as Adder, Integrator and Differentiator

Components: Op-Amp μA 741, Resistors, Capacitor, Signal Generator, CRO, Fixed Power supply +12V,0,-12V.

a) Op-Amps as summer(Inverting)

Circuit Diagram:



Design :

Design a summing amplifier to obtain a output of –6V. Since inputs are given to Inverting terminal, output is given by,

$$V_0 = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

- Let $R_f = R = R_1 = R_2 = R_3 = 1K$ and $R_4 = R_5 = R_6 = 1K$

Applying voltage divider method to the circuit

$V_1 = V_{in}$;

$$V_2 = \frac{(R_5 + R_6)Vi_n}{R_4 + R_5 + R_6} = 2/3\ V_{in}$$

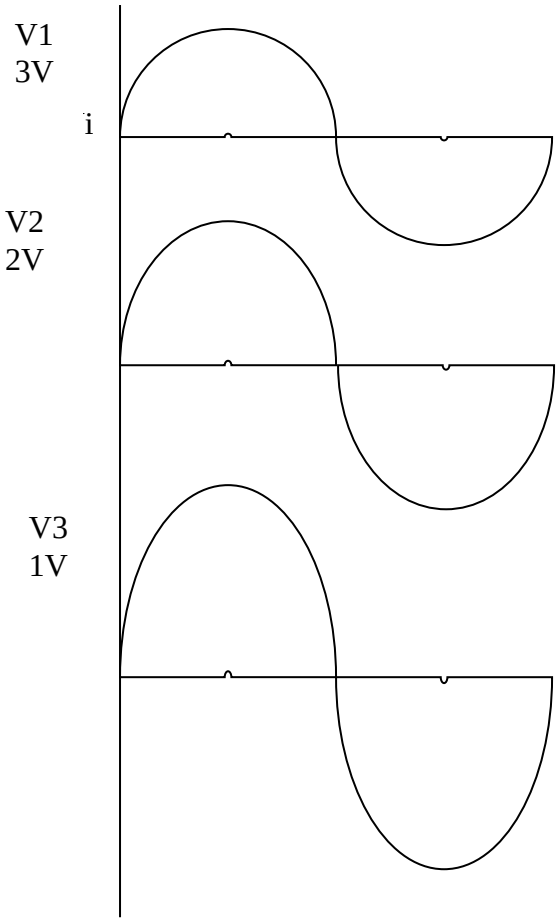
$$V_3 = \frac{(R_6)Vi_n}{R_4 + R_5 + R_6} = 1/3\ V_{in}$$

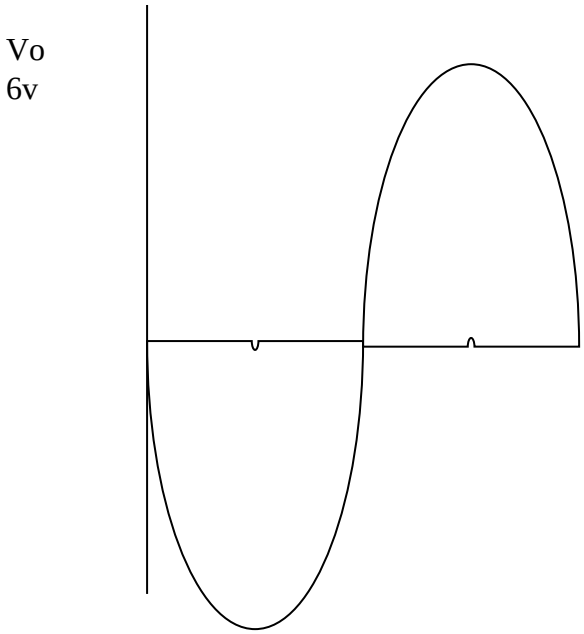
Procedure :

- Connections are made as shown in the circuit diagram.
- With the chosen values of R_f, R_i, and R_3, provide DC voltages V_1, V_2, and V_3 from VRPS.
- Measure the output voltage and compare it with the designed value.
- Repeat the above procedure providing AC sinusoidal signal of frequency 1KHz for V_1, V_2 and V_3 and observe the output waveform.

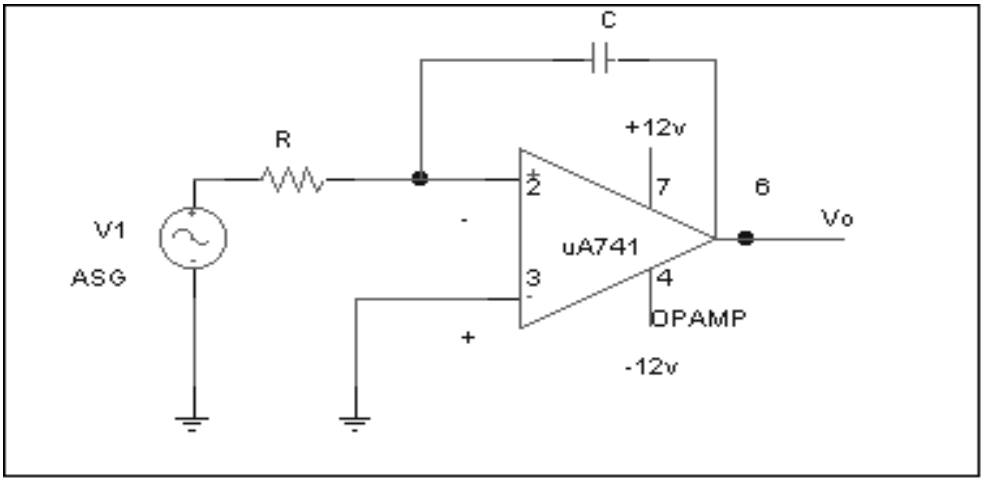
Expected waveforms:

For AC inputs:





b) Op-amp as a integrator:
Circuit Diagram:



Design :

Design a integrator circuit for different values of R and C. Since input is given to Inverting terminal, the output of integrator is given by

$V_0 = (1/RC)\int Vi.dt$

Note: Requirement for integration is RC>>T, where T is the time period of input signal. Consider input square wave of frequency 1 KHz

$\therefore$ T = 1/f= 1 ms

Since RC >> T, let RC = 10 T = 10ms

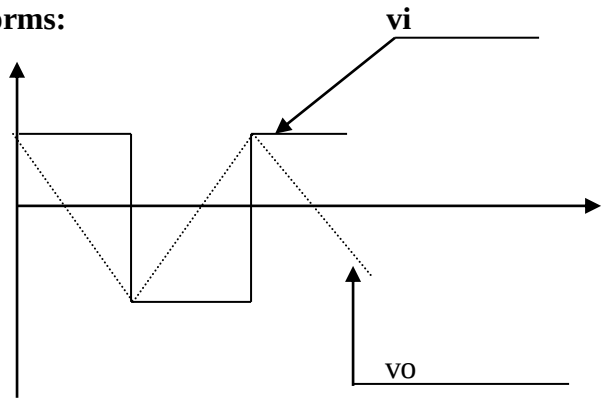
For C = 0.1 μf, R = (10*10ms)/C = 100KΩ

Choose,R = 100KΩ and C = 0.1 μf

Procedure:

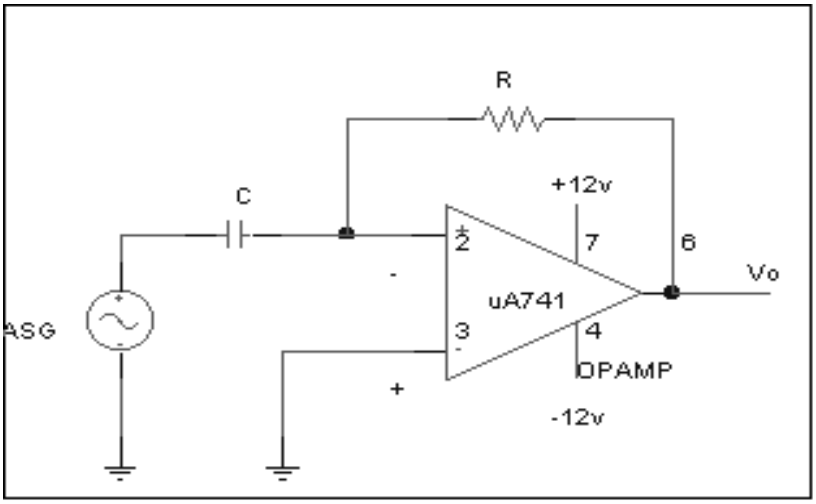
- Connections are made as shown in the circuit diagram.
- The input square wave signal (V_i) is set to 4V(p-p) of 1KHz frequency.
- For the chosen values of Rand C, Observe the output Waveform (V_o) on the CRO and verify it with the expected waveforms.
- Repeat the experiment for different values of R and C (RC = 10T, RC = T, RC=0.1T).

Expected waveforms:



c) Op-amp as a differentiator:

Circuit Diagram:



Design :

Design a differentiator circuit for different values of R and C. Since input is given to inverting terminal, the output of differentiator is given by

$$V_o = -RC\frac{dVi}{dt}$$

Note: Requirement for integration is RC<< T, where T is the time period of input signal. Consider input square wave of frequency 1 KHz

$$T = \frac{1}{f} = 1 \text{ ms}$$

Since RC << T, let RC = $\frac{1}{10}T$ = 0.1 T

for C = 0.1 μf

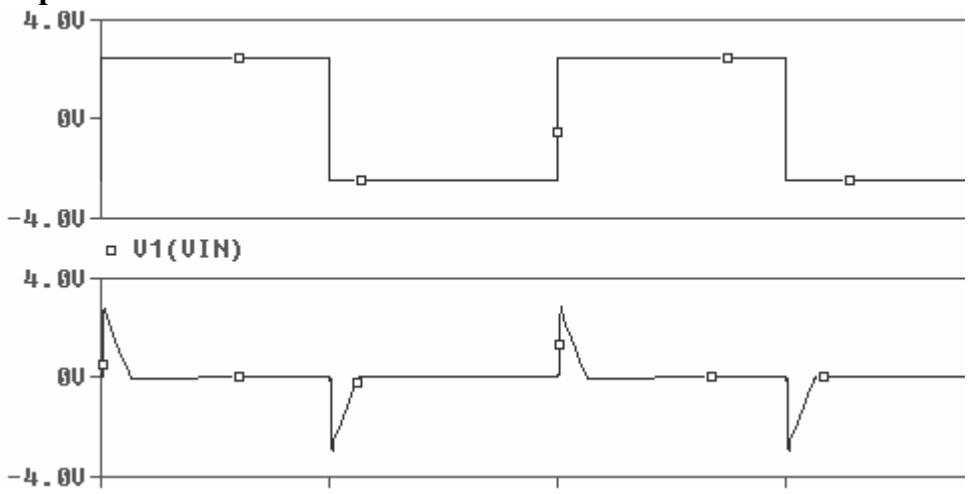
$$\therefore R = \frac{0.1\times10^{-3}}{0.1\times10^{-6}} = 1K\Omega$$

choose, R = 1KΩ and C = 0.1 μf

Procedure :

- Connections are made as shown in the circuit diagram.
- The input square wave signal (V_i) is set to 4V(p-p) of 1KHz frequency.
- For the chosen values of Rand C, Observe the output Waveform (V_o) on the CRO and verify it with the expected waveforms.
- Repeat the experiment for triangular waveform.
- Repeat the experiment for different values of R and C (RC = 10T, RC = T, RC=0.1T).

Expected waveforms:



EXPERIMENT-6

6(a)Voltage comparator and Zero crossing detector

Aim: To verify the operation of an op – amp as voltage comparator and zero crossing detector.

Procedure:

1. Connect the circuit as shown in the figure

2. Apply the supply voltages of +15V to pin 7 and -15V to pin 4 of IC 741 respectively from IC Trainer kit. Connect the ground to the ground point.

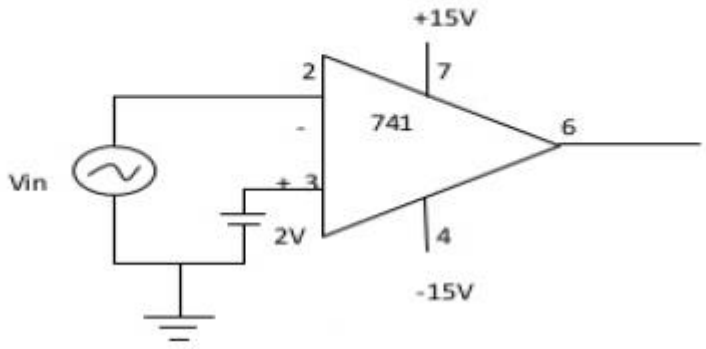
3. Set the reference voltage as 1V DC.

4. Apply sine wave of 10Vp-p with1KHz frequency from the function generator as Vi.

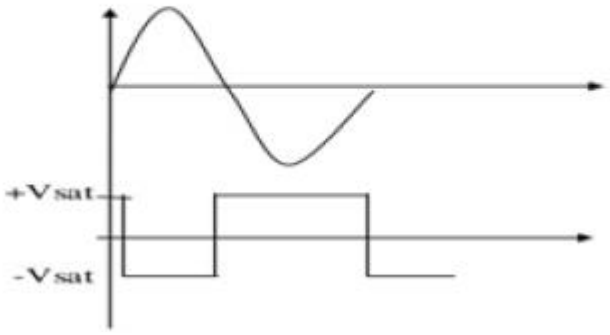
5. Check the output in CRO and calculate the amplitude of the output wave form.

6. Compare the output wave form amplitude with input signal amplitude.

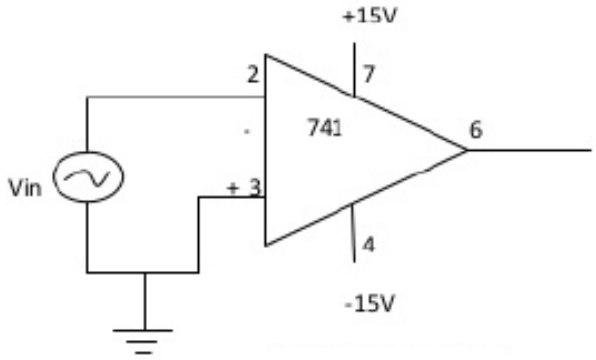
(a) Voltage comparator circuit



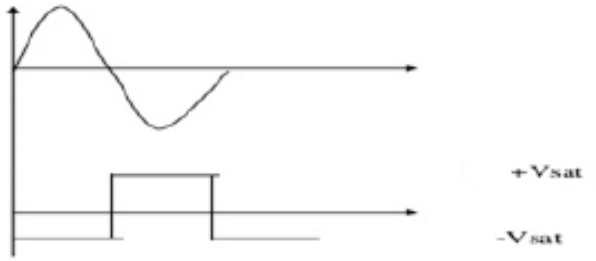
Wave forms:



(b) Zero crossing detector.



Wave forms:



Result:

Thus the function of comparator is studied and output waveform has been observed.

6(b).SCHMITT TRIGGER

Aim : To design a Schmitt trigger circuit for the given specifications and hence to plot its output
wave form and transfer characteristics.

APPARATUS REQUIRED
1. OPAMP-741
2. RESISTORS
3. BOARD AND
CONNECTING WIRES

Procedure :
1. Connections are made as shown in the circuit diagram.

2. A sinusoidal input whose amplitude is greater than the magnitude of the UTP & LTP is applied, a square wave output is obtained and observed on the CRO.

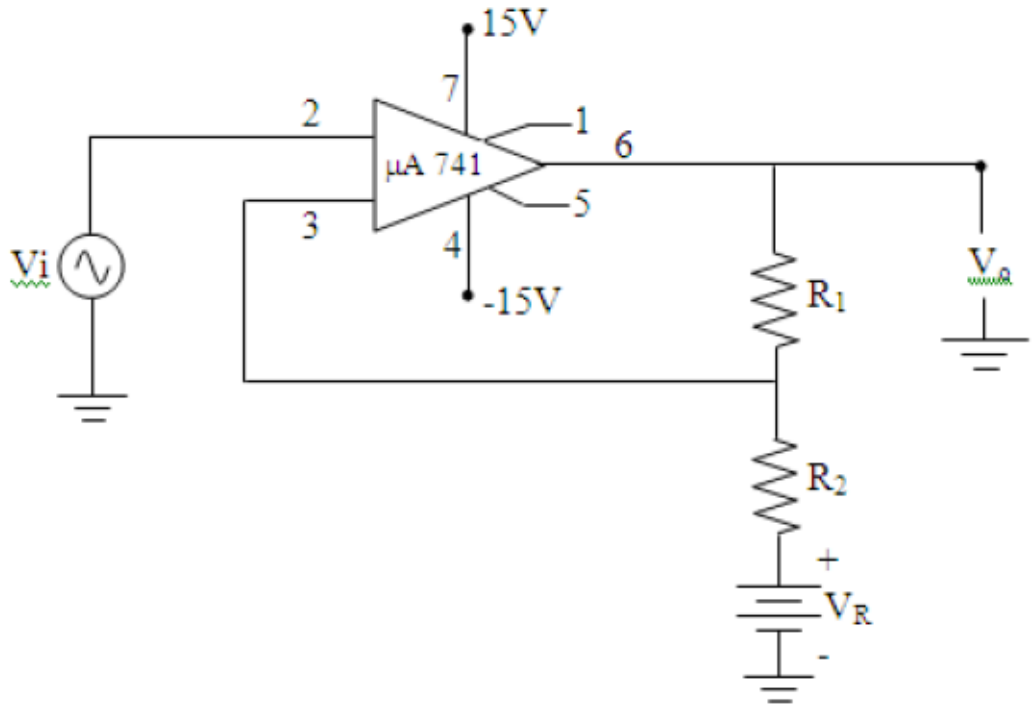
3. UTP & LTP points are noted.

4. To obtain transfer characteristics, input is applied to channel A and output to channel B.

5. UTP & LTP are measured on the transfer characteristics.

Note : The amplitude of the input voltage should be greater than the magnitude of UTP & LTP level.

Circuit Diagram:



Design :

Specifications :UTP = 6V, LTP = **-2V**

$$UTP = 6 = \frac{V_R R_1}{R_1 + R_2} + \frac{V_{sat} R_2}{R_1 + R_2} \text{-------}(1)$$

$$LTP = -2 = \frac{V_R R_1}{R_1 + R_2} - \frac{V_{sat} R_2}{R_1 + R_2} \text{-----}(2)$$

$$(1)-(2) \Rightarrow UTP - LTP = 8 = 2\frac{V_{sat} R_2}{R_1 + R_2} \text{--------}(3)$$

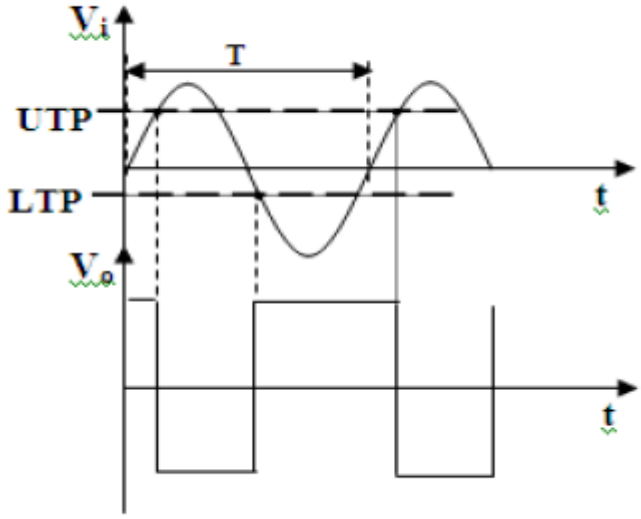
$$(1)+(2) \Rightarrow UTP + LTP = 4 = 2\frac{V_R R_1}{R_1 + R_2} \text{--------}(4)$$

Let Vsat = 12 V & $R_2 = 10k\Omega$

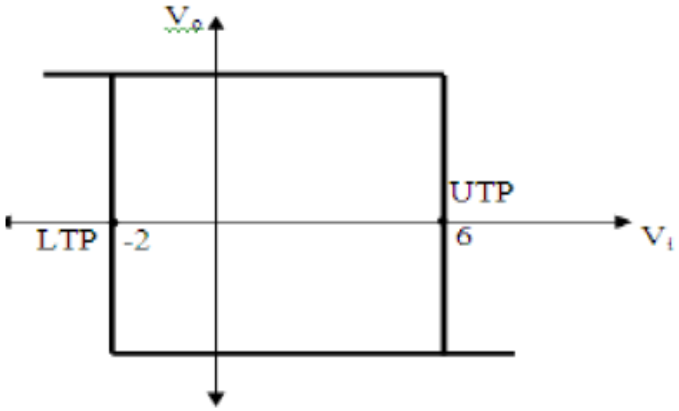
$$(3) \Rightarrow R_1 = 20k\Omega$$

$$(4) \Rightarrow V_R = 3V$$

WAVEFORMS:



TRANSFER CHARACTERISTICS:



Result :

Sl. No.	UTP		LTP	
	Theoretical	Practical	Theoretical	Practical
1.				
2.				
3.				
4.				
5.				

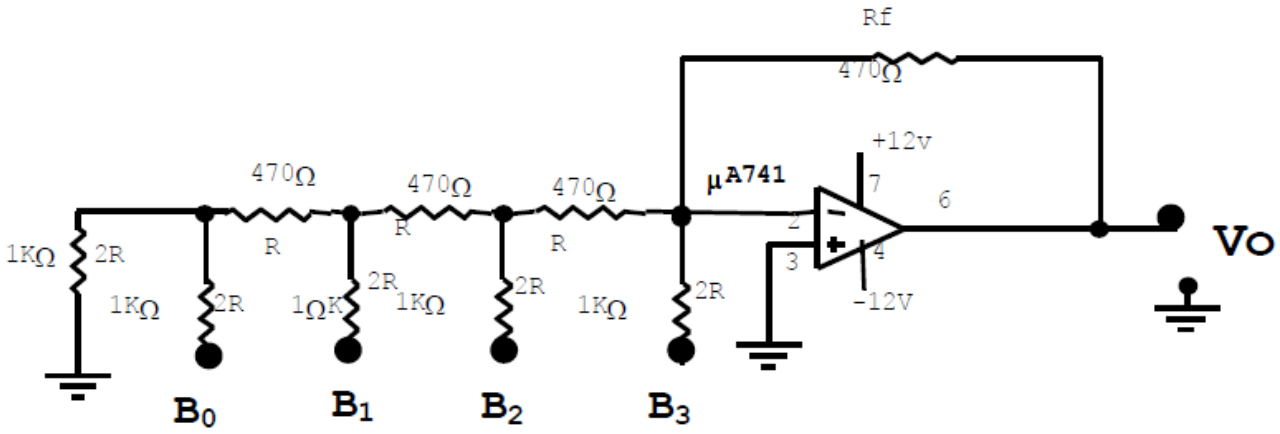
EXPERIMENT-7

4 bit R-2R Ladder Network

Aim: (a) Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches.

Components required: Op-Amp µA-741, Resistors, Signal Generator, CRO, Fixed Power supply +12V,0,-12V.

Circuit Diagram:



Design:

Choose R_f=R=470Ω

2R=2x470=1kΩ

Given n=step size=4

$$Vo = \frac{-Vref\ R_f}{2^n\ \ R}\ [B0\ 2^0+B1\ 2^1+B2\ 2^2+B3\ 2^3]$$

For example:

B0 B1 B2 B3= 1 0 0 0

$$Vo = \frac{-5\ 470}{2^4\ \ 470}\ [1x\ 2^0+0x2^1+0x\ 2^2+0x\ 2^3]$$

Vo= -0.3125V

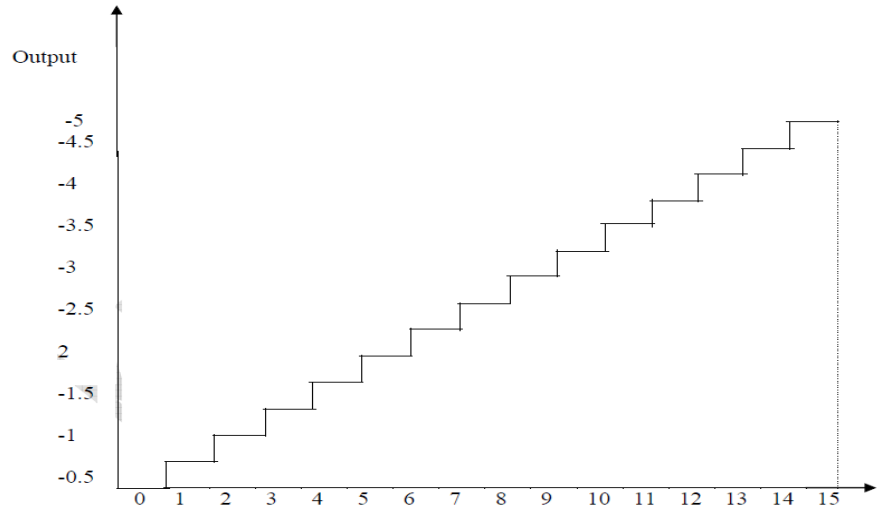
Procedure:

1. Connections are made as shown in the circuit diagram.
2. The input B0 B1 B2 B3 are connected to the input toggle switches.
3. Give the binary form (0000 to 1111) and measure the output of OP-AMP using digital multimeter and verify it with the theoretical value.
4. Plot the Graph of binary input versus the output Voltage of an OP-AMP.

Tabular Column:

Sl no	Binary Inputs				Theoretical Values	Practical Values
	B3	B2	B1	B0		
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						

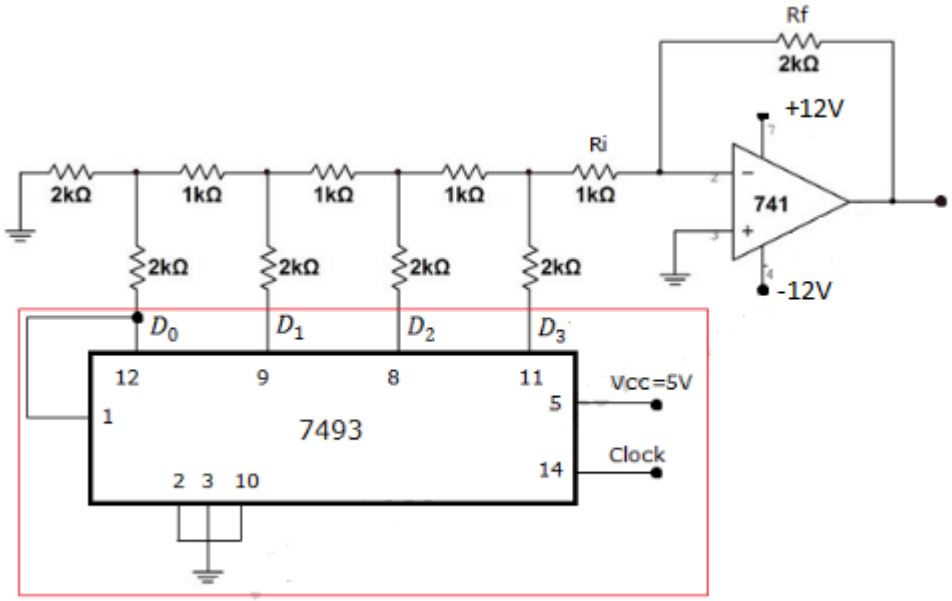
Ideal graph for binary input versus output voltage:



Aim: (b) Design 4 bit R – 2R Op-Amp Digital to Analog Converter using Mod-16 Counter

Components required: Op-Amp µA-741, IC 7493, Resistors, Signal Generator, CRO, Fixed Power supply +12V,0,-12V

Circuit Diagram:



Procedure:

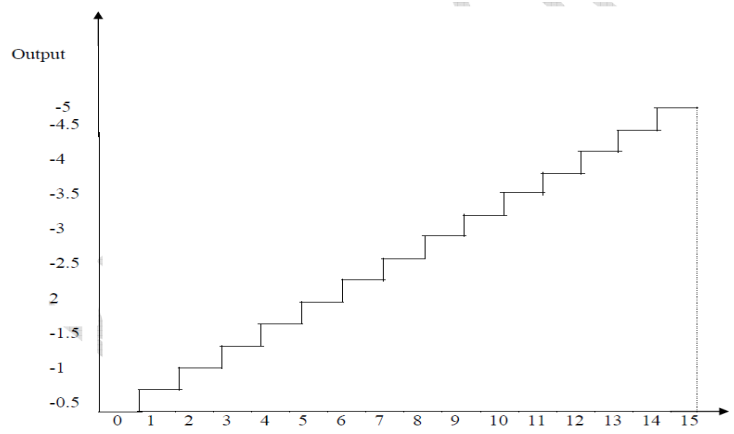
1. Connections are made as shown in the circuit diagram.
2. The input D0 D1 D2 D3 are connected to the input toggle switches.
3. Measure the output of OP-AMP using digital multimeter and verify it with the theoretical value.
4. Plot the Graph of binary input versus the output Voltage of an OP-AMP.

Tabular Column:

Sl no	Binary Inputs				Theoretical Values	Practical Values
	B3	B2	B1	B0		
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						

12						
13						
14						
15						
16						

Ideal graph for binary input versus output voltage:

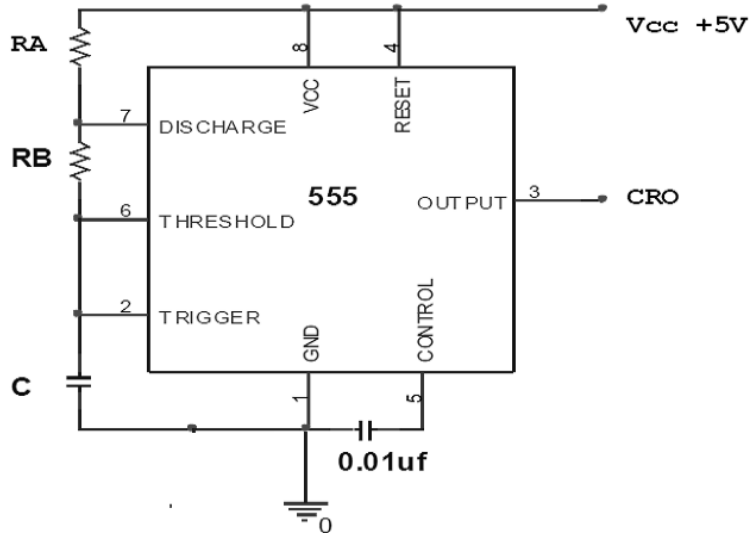


EXPERIMENT -8

Aim: - To Design of Monostable and Astable Multivibrator using 555 Timer
Components required: 555 Timer, Resistor, Capacitor, Power supply +5V, 0, CRO.

a) <u>Astable Multivibrator (free running oscillator)</u>: -

Circuit:



Design: -

Output time period of oscillations = $T=T_{on} + T_{off}$

Charging time Ton = 0.693 (R_A+R_B) C1

Discharge time T_{off} = 0.693 R_B.C1

Duty cycle D = $\frac{Ton}{Ton+Toff} = \frac{Ton}{T}$ =0.75

Let T = $\frac{1}{f} = 1msce,$

T_{off} = 0.693 R_B.C1

$0.25x10^{-3} = 0.693\ R_B\ x0.1x10^{-6}$

R_B = 3.6 KΩ choose as **3.3 KΩ**

Ton = 0.693 (R_A+R_B) C1

$0.75x10^{-3} = 0.693\ (R_A + 3.3\ K)\ x0.1x10^{-6}$

R_A=**7.2 KΩ choose as 6.8 KΩ**

Here V_{LT} = Lower threshold voltage = $V_{cc}/3$ = 1.66V

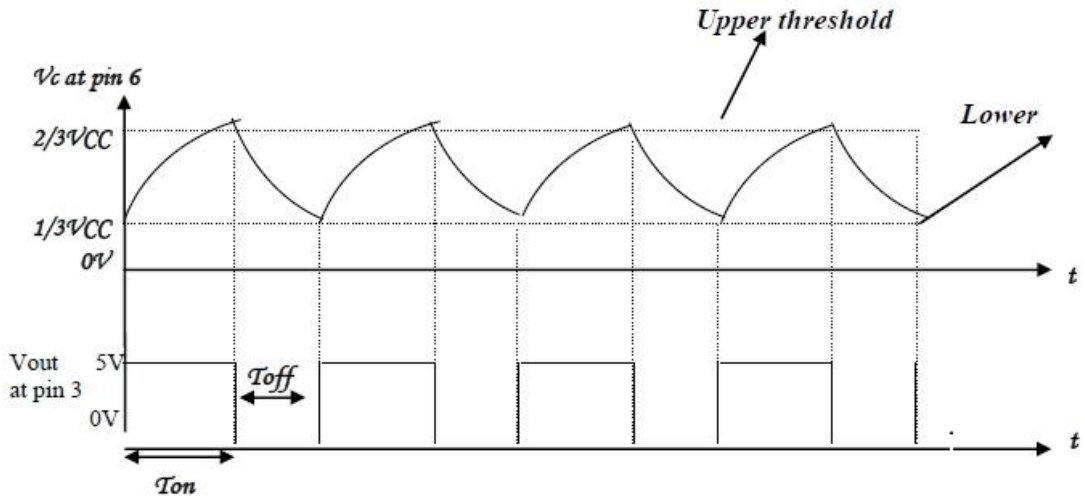
V_{UT} = Upper threshold voltage = 2Vcc/3 = 3.33V

Procedure: -

1. Connections are made as shown in the circuit diagram

2. Switch on the DC power supply unit
3. Observe the wave form on CRO at pin 3 and measure the o/p pulse amplitude and also measure Ton & Toff.
4. Observe the waveforms across C1 (Vc) & measure the max & min voltage levels & verify V_{UT} & V_{LT}.
5. Compare the capacitor voltage Vc with the output waveform Vo & note that capacitor charges & Vc rises exponentially when output is high, the capacitor C1 discharges through R_B & the discharge transistor & Vc falls exponentially when output is low.
6. Calculate the duty cycle & the output frequency f & verify with the designed values.

Waveform:



Tabular Column:

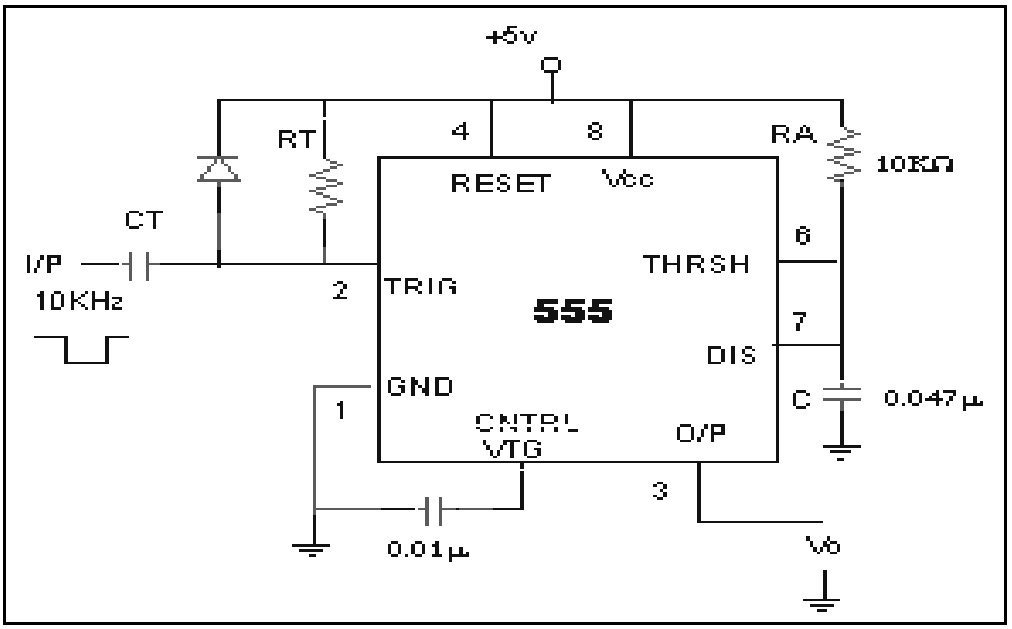
Parameters	Theoretically	Practically
Frequency		
Duty cycle		
Ton		
Toff		
$V_{LT} = V_{cc}/3$		
$V_{UT} = 2Vcc/3$		

Result: - Designed values are verified**.**

b) Monostable Multivibrator circuits Using 555 Timer.

Components required: Op-Amp μA 741, Capacitor, Function Generator
Fixed Power supply +12V,0,-12V, CRO.

Circuit:



Design:

Let output pulse width = Delay time t_d 0.5 msec

Output delay time $T_d = 1.1\ R_A.C$

Let $R_A = 10\ K\Omega$ Then

$$C = \frac{T_d}{1.1R_A} = 0.045\,\mu F \qquad (Use\ 0.047\,\mu F \text{ standard } capacitor)$$

Here $V_{UT} = \frac{2}{3}V_{CC}$ = upper threshold voltage

Choose $R_T C_T << T_d$

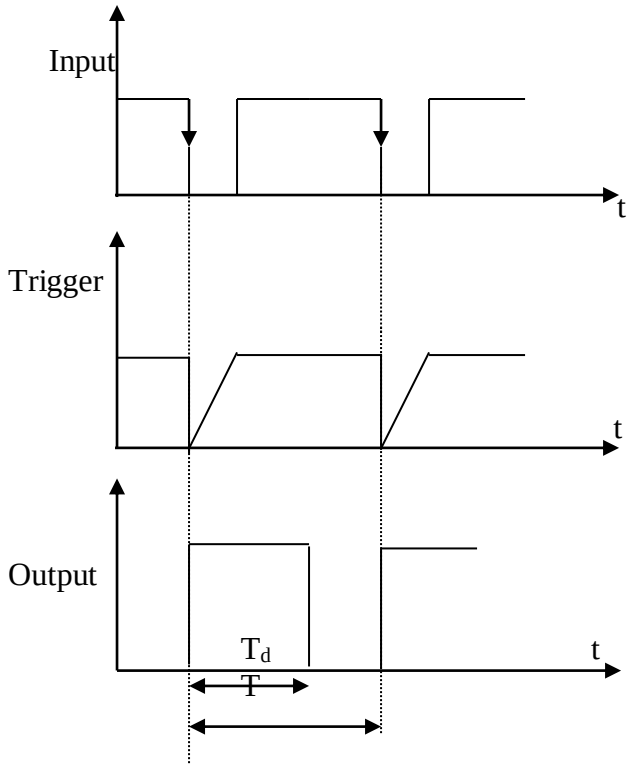
Select $R_T C_T << \frac{T_d}{10}$

Output duty cycle $d = \frac{T_d}{T}$ $\quad \because f = \frac{1}{T} =$ Input trigger pulse frequency

Adjust input frequency 'f ' from the pulse generator to f = 1KHz

i.e., T = 1ms (i.e., twice the output delay time

Waveforms: -



Input Trigger pulses

Voltage waveform at pin no.2

Output voltage at pin 3

Procedure: -

1. Connections are made as shown in Figure

2. Switch on the power supply and observe the output waveforms on CRO at pin no 3 and measure the output delay time T_d and verify with the designed values and also observe the waveforms at pin no 2 – trigger input terminal & at pin no 7, also measure the voltage levels.

Result: -

Output delay time is verified.

SOFTWARE EXPERIMENTS:

EXPERIMENT 1

NARROWBAND PASS AND NARROW BAND REJECT FILTER:

Aim

The frequency response of a narrow-bandwidth active band-pass filter will be measured and the results will be compared to theoretical expectations.

Software Used:

MULTISIM 3.0

Theory:

The operational amplifier band-pass filter circuit on the right uses a high-pass and a low-pass filter section to obtain a band-pass response.

The RC network, R2 and C2, in its negative feedback path provides the low-pass portion of the band-pass response.

Series connected C1 and R1 provide the high- pass portion.

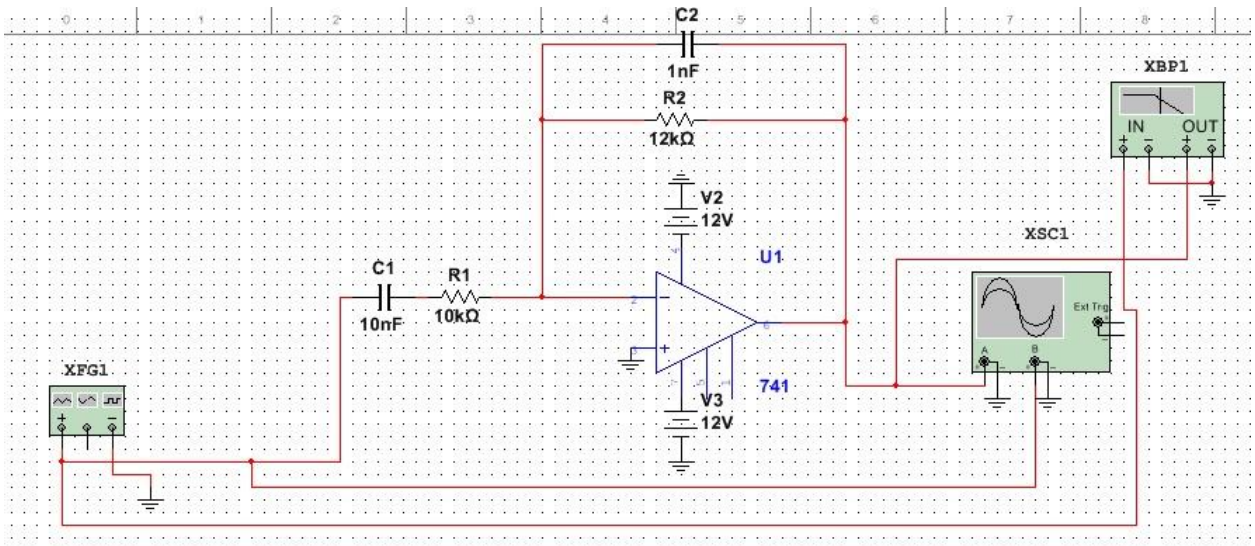
This circuit has a typical second order resonant response of the form:

$$H(s)=\frac{K s}{s^2+\beta s+\omega_o^2} \qquad \beta = bandwidth \qquad \omega_o = resonant\ frequency$$

$$\frac{0-Vin}{R1+\frac{1}{sC1}}+\frac{0-Vout}{R2}+\frac{0-Vout}{\frac{1}{sC2}}=0 \qquad H(s)=\frac{-s\frac{1}{C2R1}}{s^2+s\left(\frac{1}{C1R1}+\frac{1}{C2R2}\right)+\left(\frac{1}{C1R1}\right)\left(\frac{1}{C2R2}\right)}$$

$$H(j\omega)=\frac{-j\omega K\omega_2}{\left(\omega_o^2-\omega^2\right)+j\omega\left(\omega_1+\omega_2\right)} \qquad K=\frac{R2}{R1} \qquad \omega_1=\frac{1}{C1R1} \qquad \omega_2=\frac{1}{C2R2} \qquad \omega_o^2=\omega_1\omega_2$$

Gain when $\omega=\omega_o$: $A_V=\frac{K\omega_2}{\left(\omega_1+\omega_2\right)}$

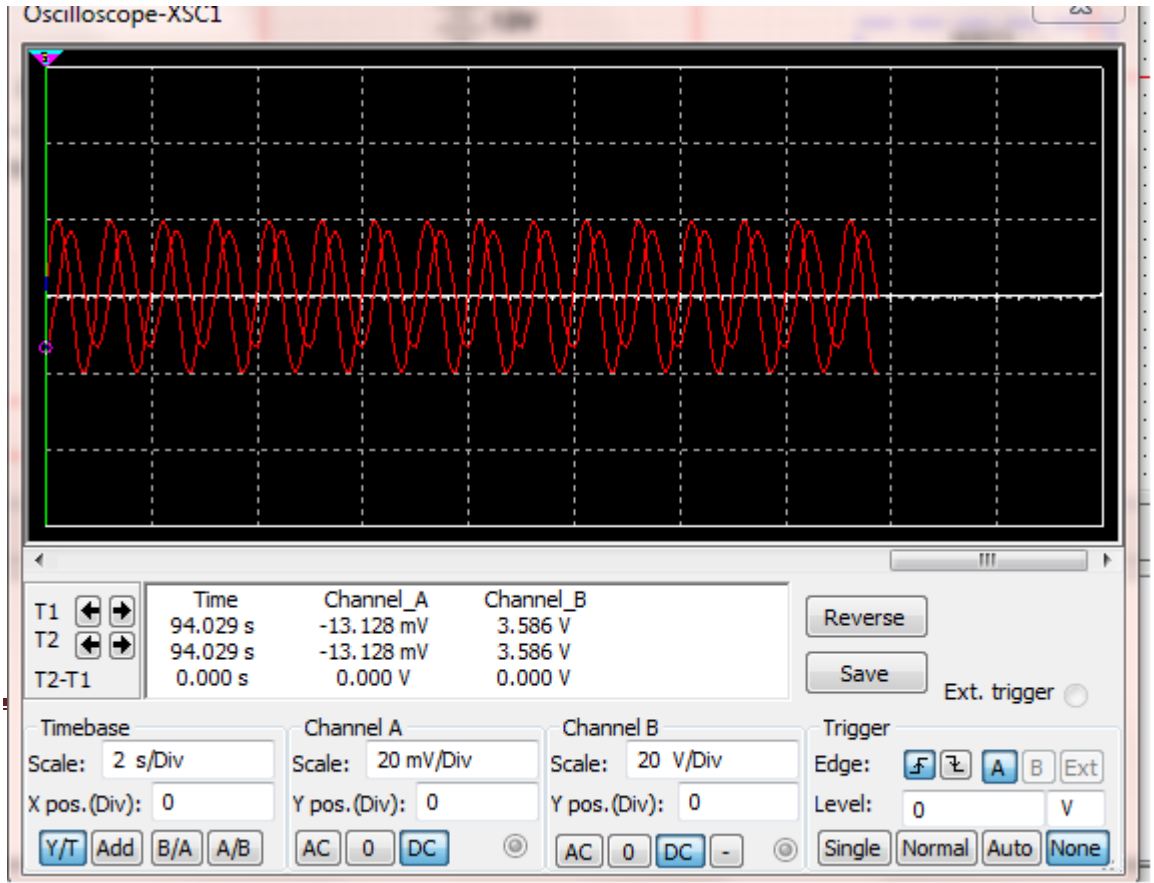


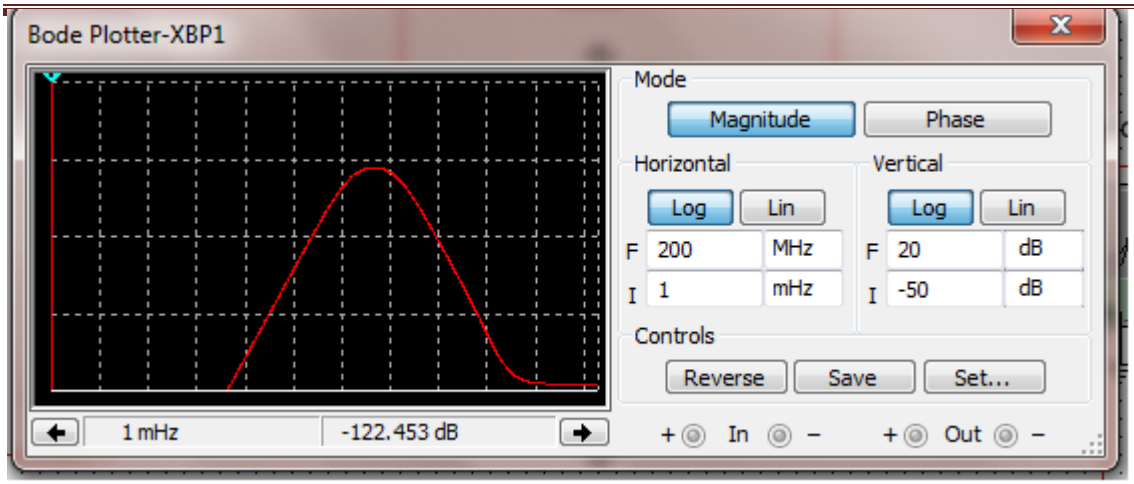
It is important to note that the bandwidth of this filter is the sum of the cutoff frequencies of the individual sections:β=ω1-ω2 and not β=ω1+ω2
The bandwidth does approach the traditional definition of bandwidth, when the cutoff frequencies are over a decade apart. B=ω1-ω2
The actual cutoff frequencies are the frequencies where the magnitude of the filter's transfer function is equal to -3 dB of its maximum value. The theoretical values of these frequencies are most easily found by simulation. Solutions using Maple are also provided in the analysis section of this experiment.

Frequency and Bandwidth Calculations

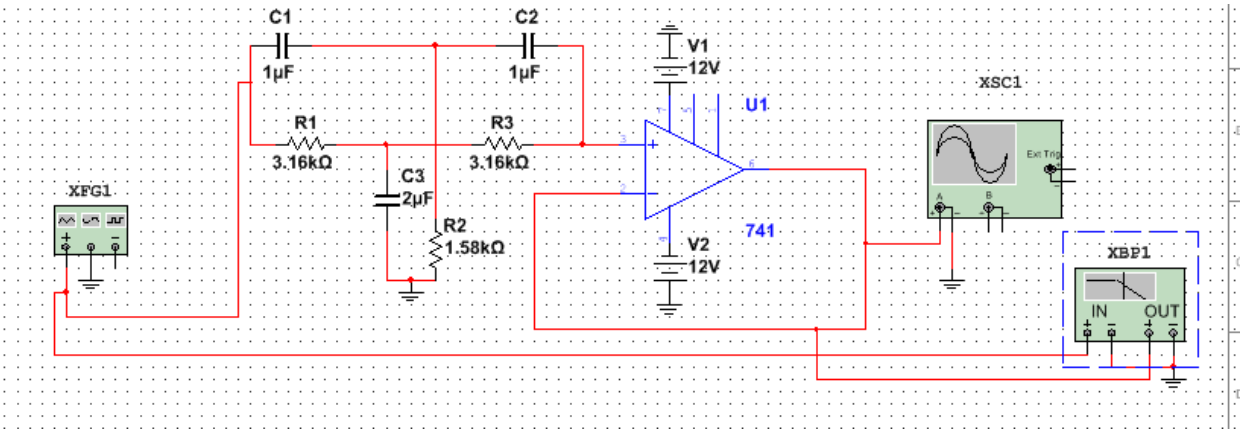
Given: w1 = 1/R1C1 and w2 = 1/R2C2. K = R2/R1. Calculations below are for w1 = 10 and w2 = 100. Input w1 and w2 for your filter. calculate the filter's cutoff frequencies

Result:





Narrow Band Reject Filter:



Step 1: select notch frequency that is the frequency to be rejected. Mostly such filters are used to remove power line frequency that is 50 Hz. So take Fn = 50 Hz

Step 2: assume capacitor value C as 1 micro F (because frequency is too low the capacitor value should be large)

Step 4: calculate value of R from

$$Fn = 1 / 2\pi RC$$

$$R = 1 / 2\pi FnC$$

$$= 1 / 2 \times 3.14 \times 50 \times 10^{-6}$$

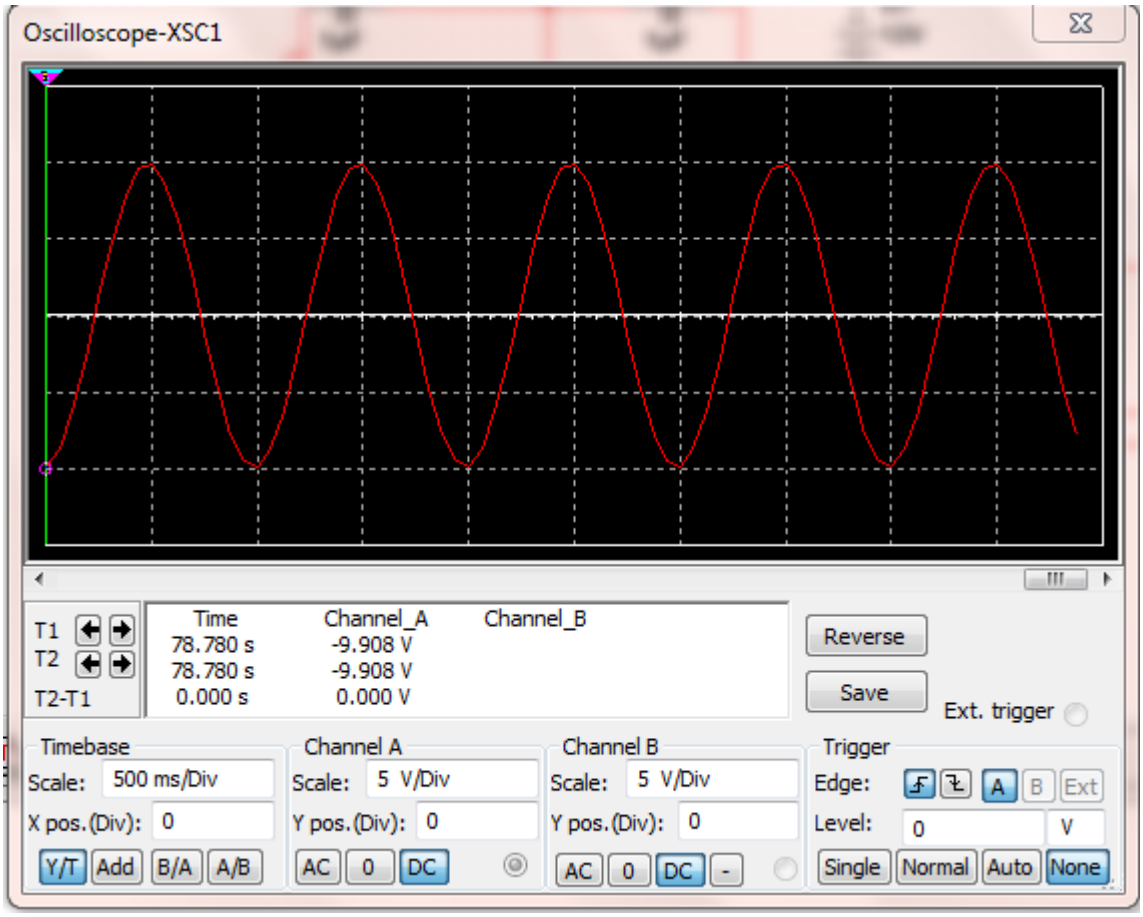
$$= 3180\ \Omega$$

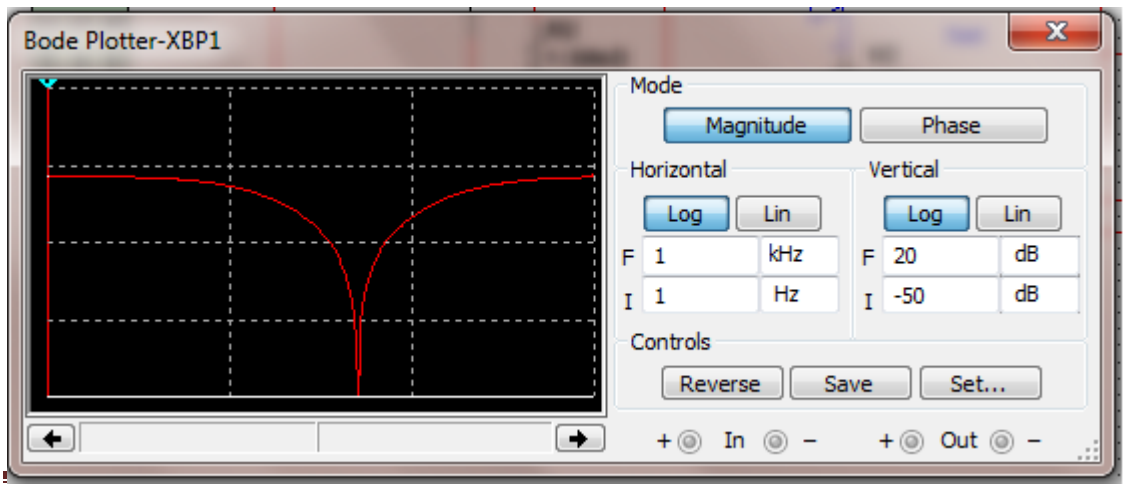
Fig. 5: Screenshot of calculations required to find resistance for Notch Filter

Step 5: to construct T network with C – R/2 – C, we need R/2 value. So connect two resistors in parallel of same value R

Step 6: to construct T network with R – 2C – R, we need 2C value. So connect two capacitors in parallel of same value C

Result:





EXPERIMENT 2

PRECISION HALF AND FULL WAVE RECTIFIER:
Precision Half-Wave Rectifier The Superdiode
Aim:

To simulate the half wave rectifier circuit and to check its transfer characteristics.

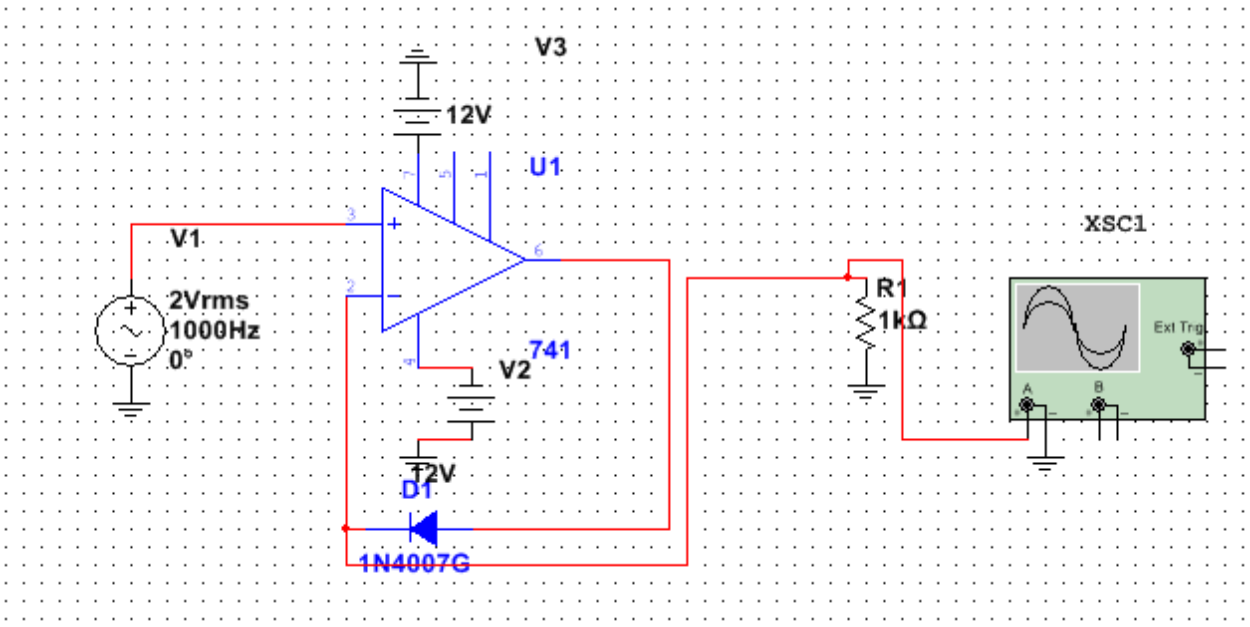
Software Used:

MULTISIM 3.0

Theory:

There are many applications for precision rectifiers, and most are suitable for use in audio circuits. A half wave precision rectifier is implemented using an op amp, and includes the diode in the feedback
loop. This effectively cancels the forward voltage drop of the diode, so very low level signals (well below the diode's forward voltage) can still be rectified with minimal error.
Components required:
Resistor=1KΩ, diode IN4007, op-amp 741

Circuit diagram:



Design:

$v_I = 10\,\text{mV} \quad v_o = 10\,\text{mV}$

$$i_D = \frac{10\,\text{mV}}{R} = 10\,\mu\text{A}$$

v_I

Given $iD = 1\,\text{mA} \quad 0.1\,\text{mA} \quad 10\,\mu\text{A}$

$v_o = 0.7\,\text{V} \quad 0.6\,\text{V} \quad 0.5\,\text{V}$

$v_I = 1\text{V} \quad v_o = 1\,\text{V}$

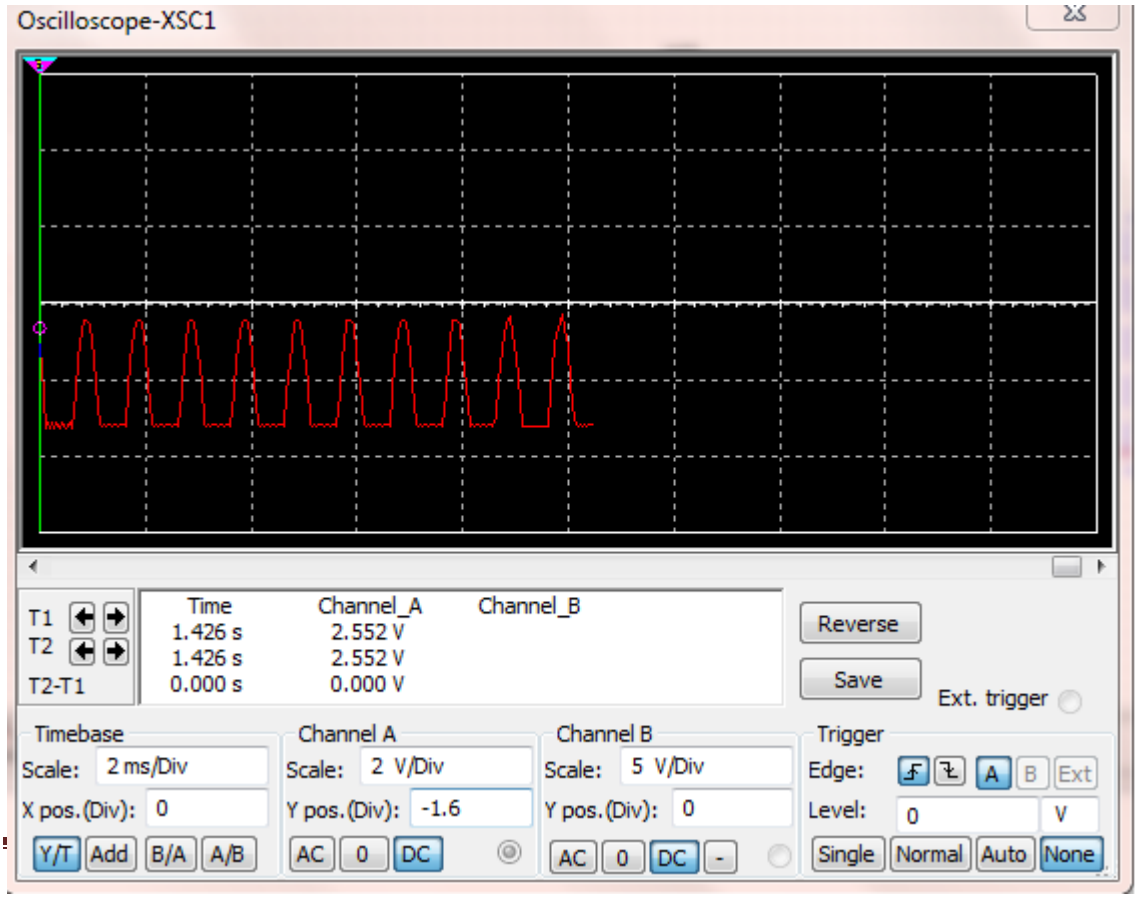
$i_D = 1\,\text{mA}, v_D = 0.7\,\text{V} \quad v_A = 1.7\,\text{V}$

$v_I = -1\text{V}$

The negative feedback loop is not operative

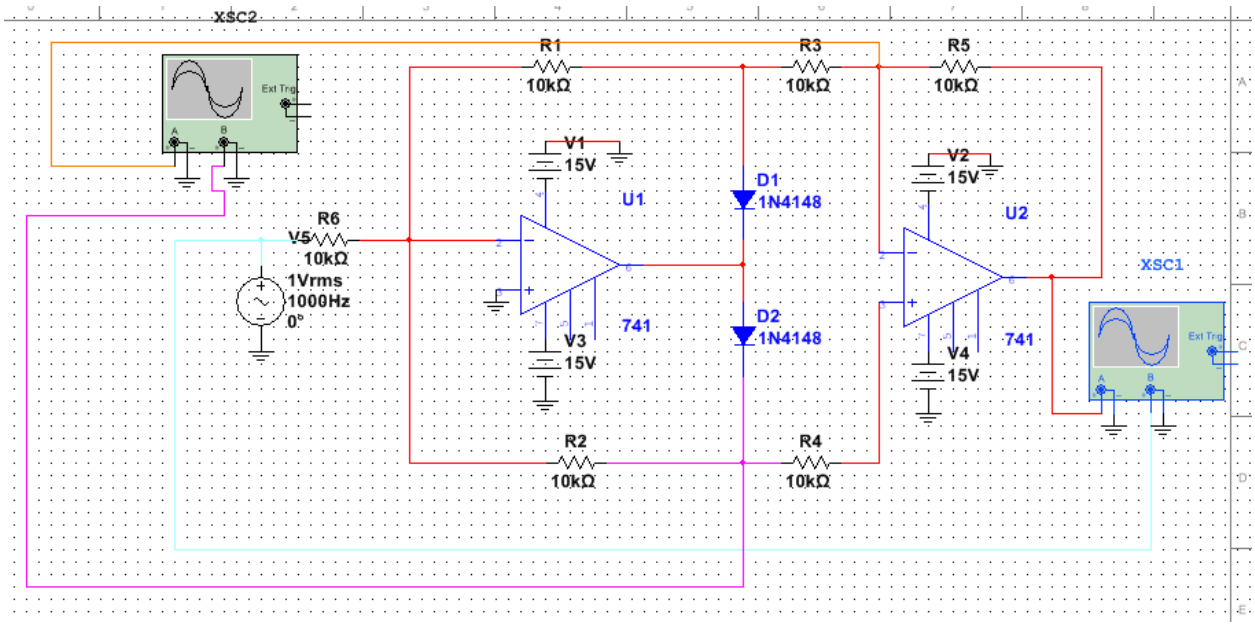
$v_o = 0\,\text{V} \quad v_A = -12\,\text{V}$

Result:



Precision Full Wave Rectifier

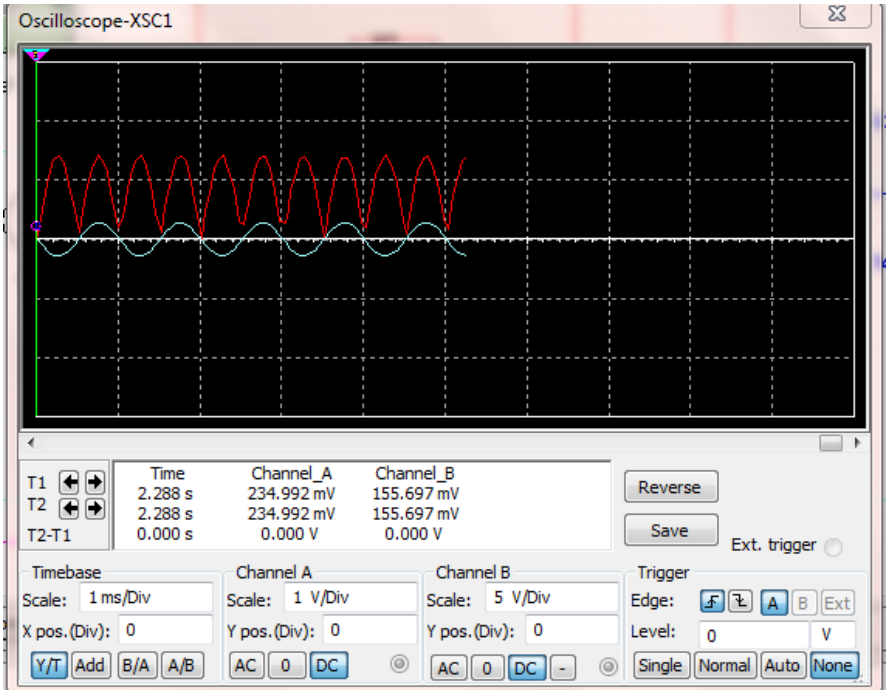
Change amplitude to 0.5 V.The plots of Vin and Vout vs time. Provide plot of Vout vs Vin. What is the peak value for the output voltage? Now modify your circuit to construct a Precision Full Wave Rectifier (Fig.4). 4.3.2 Precision Full Wave Rectifier A Precision Full-Wave Rectifier consists of superdiode DA (see Fig.3) and an inverting amp with unity gain connected to regular diode DB.



Replace DA with a superdiode and the diode DB and the inverting amplifier with the inverting precision half-wave rectifier to get the Precision Full Wave Rectifier.

Provide the plots of Vin (Vi) and Vout (Vo) vs time. Provide plot of Vout (Vo) vs Vin (Vi). What is the peak value for the output voltage? Place CL = 47 μF in parallel with RL. This will create a Peak Detector. Adjust the values of RL and CL until you achieve reasonable DC voltage level. L5: Provide peak voltage (VP) before placing the capacitor. Provide ripple voltage (VR), and dc voltage (VDC) after placing the capacitor

Result:


Oscilloscope-XSC1
T1
T2
T2-T1
Time
2.288 s
2.288 s
0.000 s
Channel_A
234.992 mV
234.992 mV
0.000 V
Channel_B
155.697 mV
155.697 mV
0.000 V
Reverse
Save
Ext. trigger
Timebase
Scale: 1 ms/Div
X pos.(Div): 0
Y/T Add B/A A/B
Channel A
Scale: 1 V/Div
Y pos.(Div): 0
AC 0 DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC 0 DC -
Trigger
Edge: A B Ext
Level: 0 V
Single Normal Auto None

EXPERIMENT 3

RC PHASE SHIFT OSCILLATOR

AIM

To setup RC phase shiftoscillator for 1 KHz and

(i) plot the output waveform

(ii) measure the frequency of oscillation

Software Used:

MULTISIM 3.0

PRINCIPLE

An oscillator is an electronic circuit for generating ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier a frequency selective network and positive feedback from the output o

the input. The Barkhausen criteria for sustained oscillator is Aβ = 1, where A is gain of the amplifier

and β is the feedback factor.

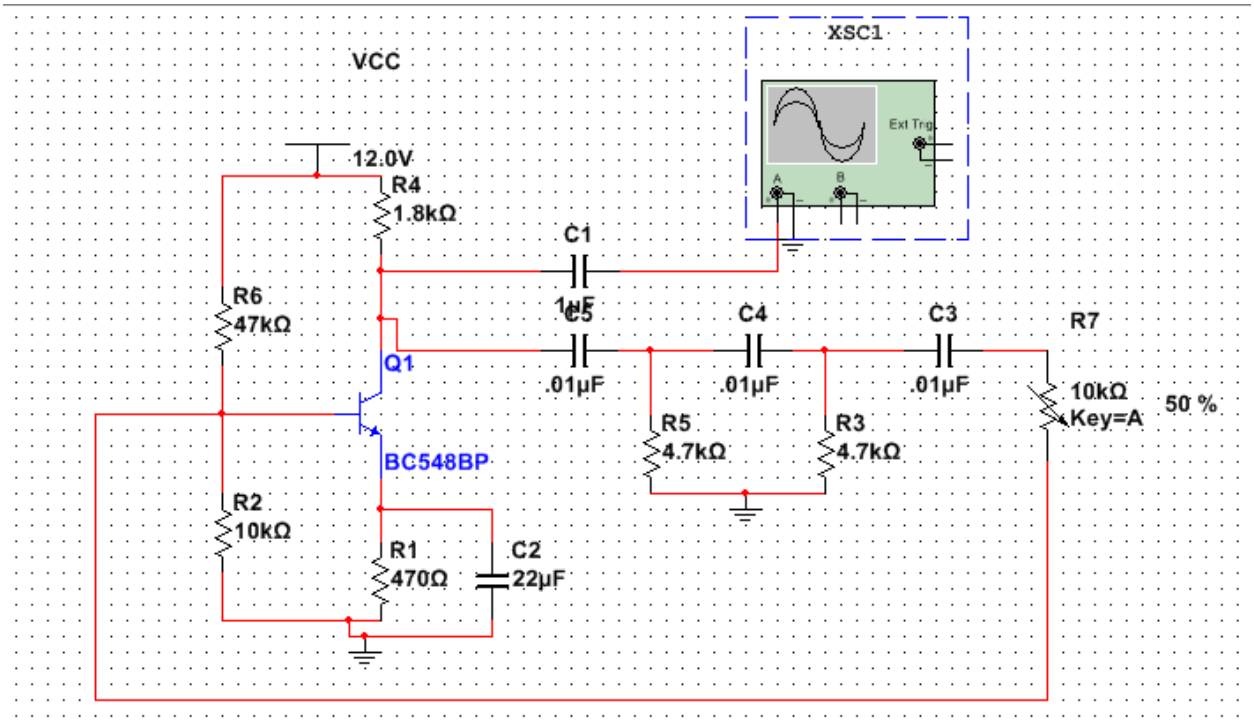
If common emitter amplifier is used with resistive collector load, there is an

180ophaseshift between input and output. The feedback network introduces an additional

180ophaseshift at a particular frequency. The three section RC network offers 180ophaseshift and the β

of . Hence for unity gain feedback, the gain of the amplifier should be 29. The phaseshift oscillator

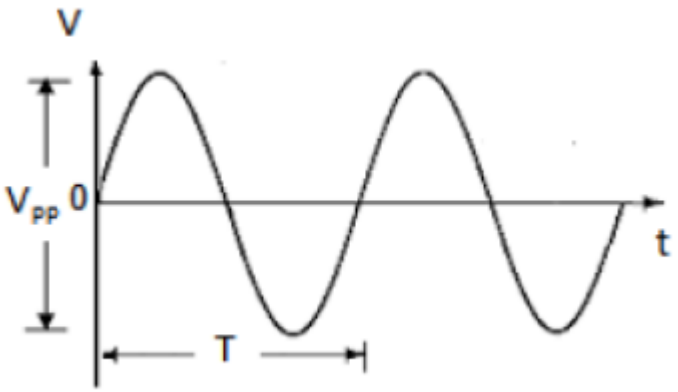
is particularly useful as audio frequency generator. The frequency of oscillation is given by .



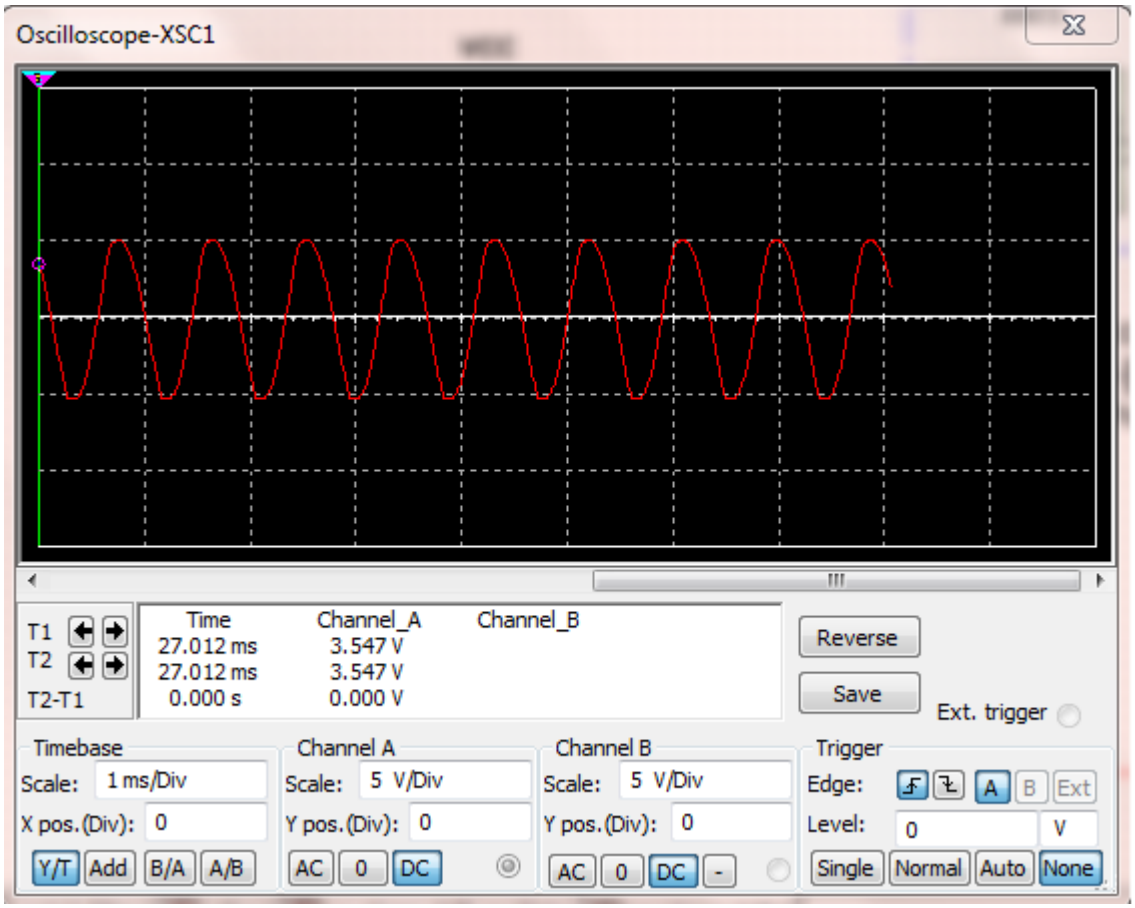
From the given component values, the frequency of oscillation

$$f = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6} \times 4.7 \times 10^{3} \times 0.01 \times 10^{-6}} =$$

Model graph:



Result:



HARTLEY OSCILLATOR

AIM:

To design and set up a Hartley oscillator using BJT and to observe the sinusoidal output waveform.

APPARATUS REQUIRED:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Transistor	BC 107	1
2.	Resistors	2.74 KΩ, 1.76KΩ,10.58KΩ	1,2,1
3.	Capacitors	0.1μF, 0.1μF	Each 2
4.	Inductor	0.1mH,0.33mH	Each 1
5.	RPS	±12V	1
6.	CRO	1MHz	1
7.	Connecting wires	-	Req.

THEORY:

The **Hartley oscillator** is an electronic oscillator circuit in which the oscillation frequency is determined by a tuned circuit consisting of capacitors and inductors, that is, an LC oscillator. The Hartley oscillator is distinguished by a tank circuit consisting of two series-connected coils (or, often, a tapped coil) in parallel with a capacitor, with an amplifier between the relatively high impedance across the entire LC tank and the relatively low voltage/high current point between the coils. The Hartley oscillator is the dual of the Colpitts oscillator which uses a voltage divider made of two capacitors rather than two inductors. Although there is no requirement for there to be mutual coupling between the two coil segments, the circuit is usually implemented using a tapped coil, with the feedback taken from the tap, as shown here. The optimal tapping point (or ratio of coil inductances) depends on the amplifying device used, which may be a bipolar junction transistor.

DESIGN PROCEDURE:

Select a appropriate transistor and note down its specification such as VCE,IC(MAX), hfe(max) and Vbe(sat).

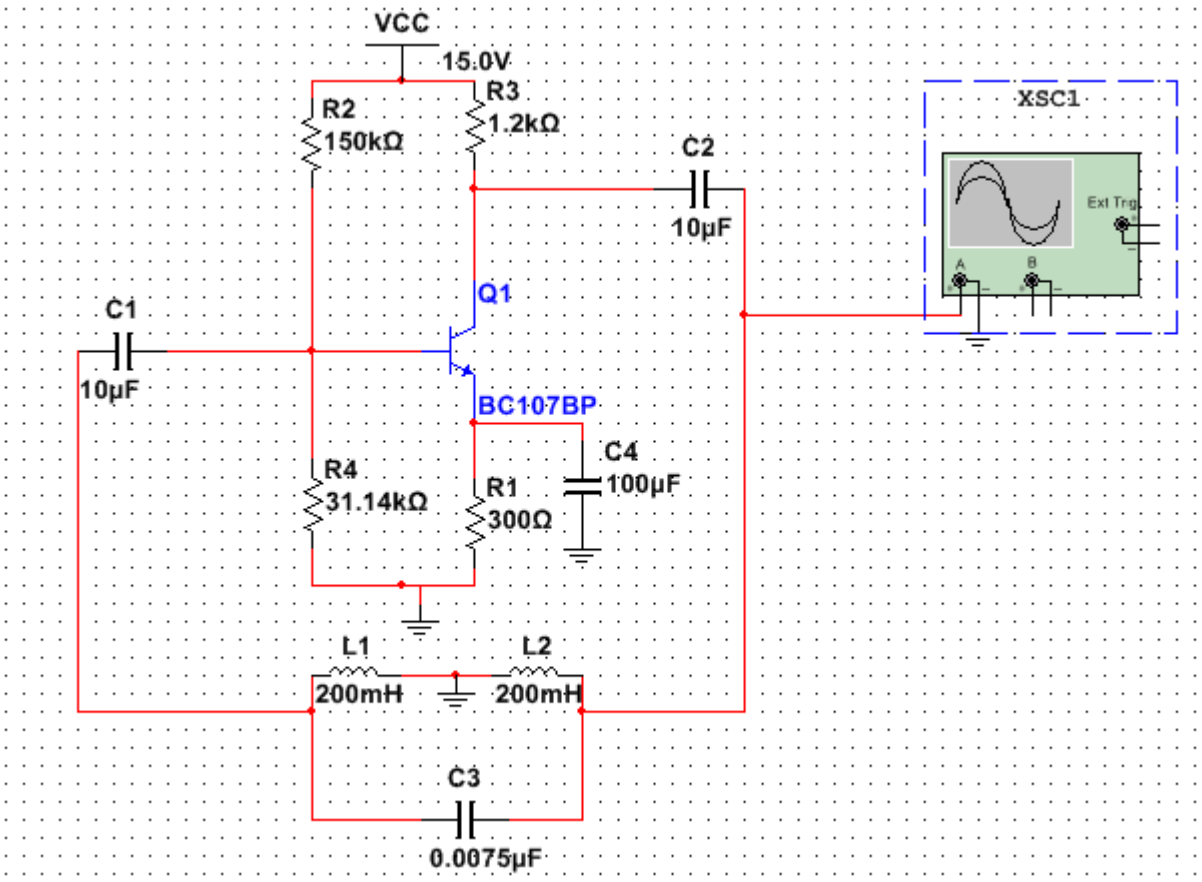
VCC= VCEQ+ ICQ(RC+RE)

R2=S* RE

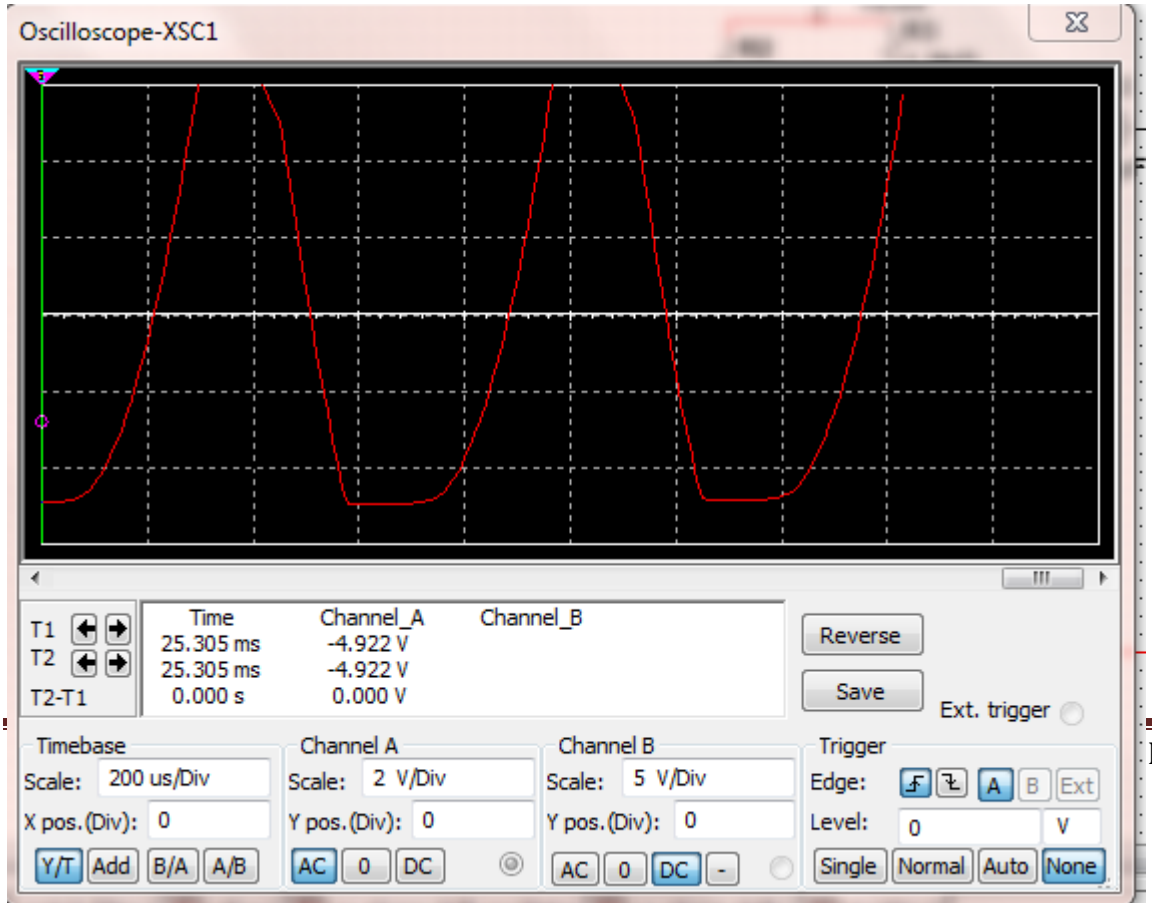
VCC[R2/(R1+ R2)= VBE+VBE(SAT)

VR1+VR2=VCC

CIRCUIT DIAGRAM


VCC
15.0V
R2
150kΩ
R3
1.2kΩ
C2
10µF
XSC1
Ext Trig
A
B
C1
10µF
Q1
BC107BP
C4
100µF
R4
31.14kΩ
R1
300Ω
L1
200mH
L2
200mH
C3
0.0075µF

MODEL GRAPH


Oscilloscope-XSC1
T1
T2
T2-T1
Time
25.305 ms
25.305 ms
0.000 s
Channel_A
-4.922 V
-4.922 V
0.000 V
Channel_B
Reverse
Save
Ext. trigger
Timebase
Scale: 200 us/Div
X pos.(Div): 0
Y/T
Add
B/A
A/B
Channel A
Scale: 2 V/Div
Y pos.(Div): 0
AC
0
DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
Trigger
Edge:
A
B
Ext
Level: 0 V
Single
Normal
Auto
None

EXPERIMENT 4

Design of Monostable Multivibrator Circuit using 555 Timer

AIM: To construct and study the operation of a monostable multivibrator using 555 IC timer.

Software Used:

MULTISIM 3.0

:

THEORY:

It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal. Let us assume that the circuit is instable state. The output V0i is at +Vsat. The diode D1 conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V,the voltage at the positive input terminal through R1R2 potentiometer divider is +ßVsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V.the output of the Op-Amp will switch from +Vsat to –Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vsat. When the capacitor charge Vc becomes slightly more negative than –ßVsat, the output of the op-amp switches back to +Vsat.

DESIGN:

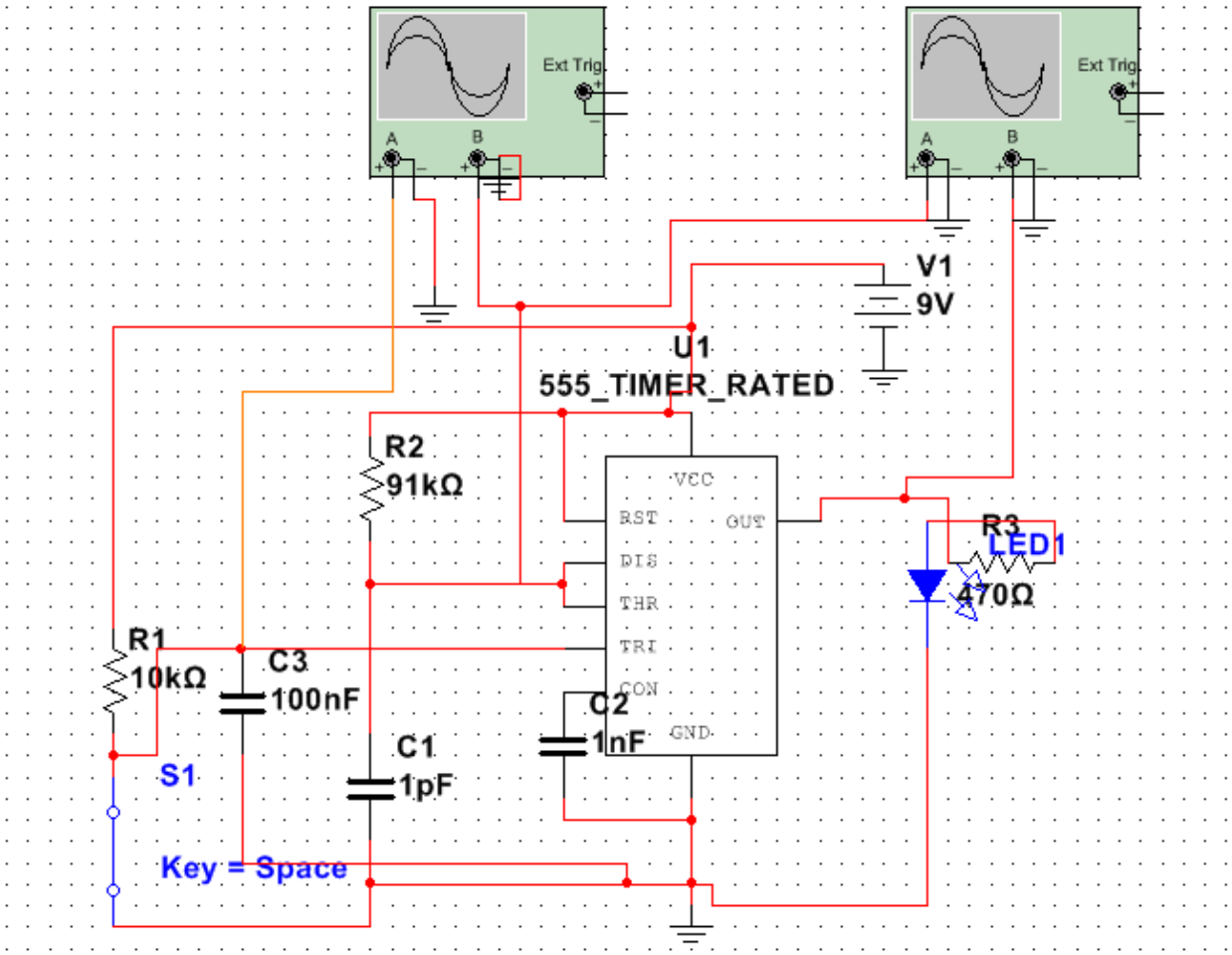
The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

$$V0 = Vf + (Vi-Vf)\, et/R \text{ , } ß = R2/(R1+R2)$$

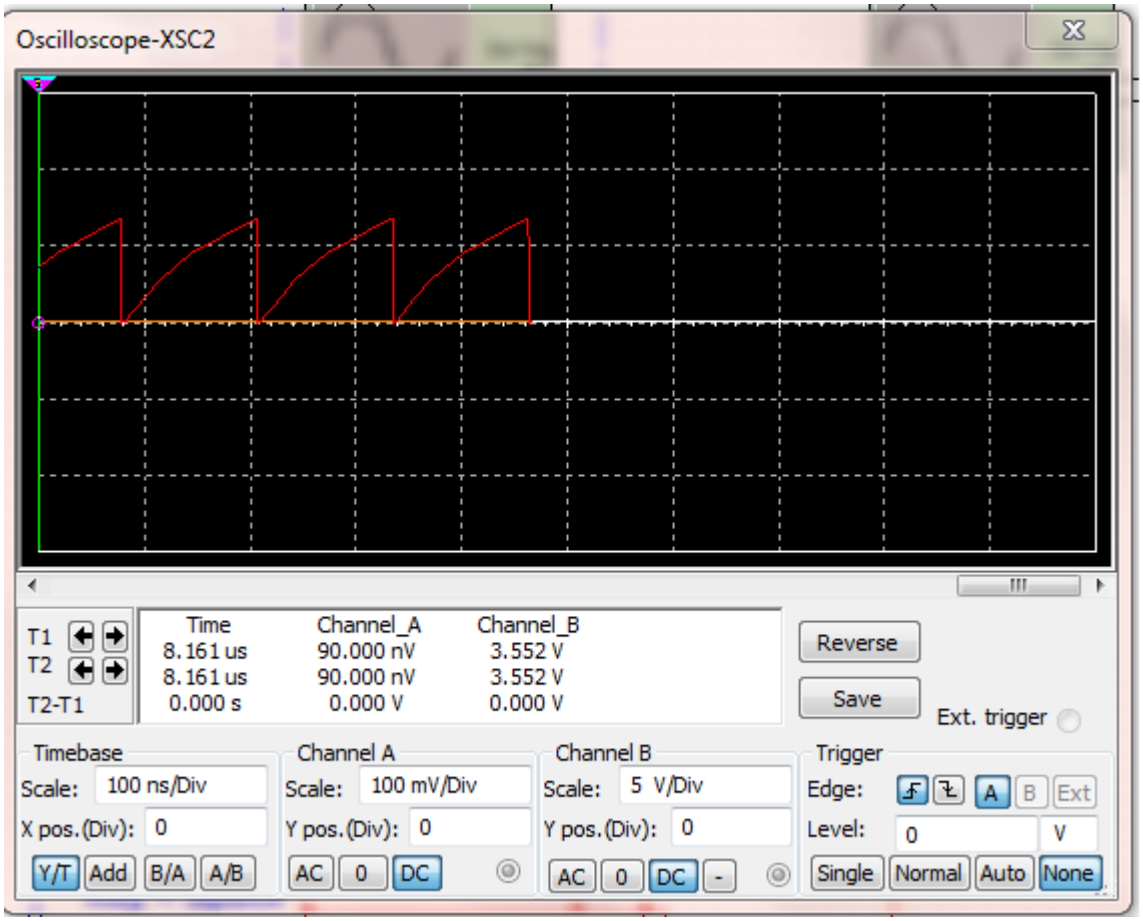
If Vsat >> Vp and R1=R2 and ß = 0.5,

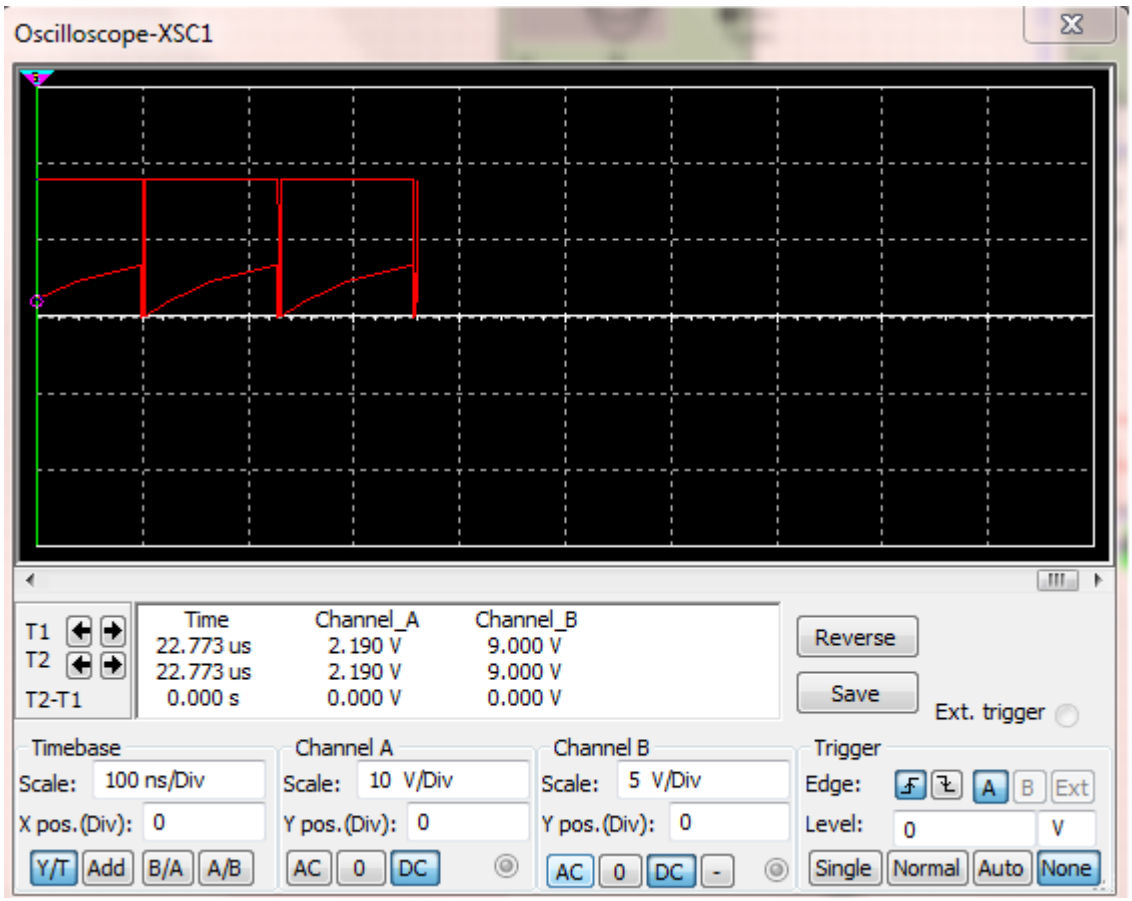
Then, T = 0.69RC

CIRCUIT DIAGRAM:



Result : The waveform is observed and verified with stated condition.


Oscilloscope-XSC2
T1
T2
T2-T1
Time
8.161 us
8.161 us
0.000 s
Channel_A
90.000 nV
90.000 nV
0.000 V
Channel_B
3.552 V
3.552 V
0.000 V
Reverse
Save
Ext. trigger
Timebase
Scale: 100 ns/Div
X pos.(Div): 0
Y/T Add B/A A/B
Channel A
Scale: 100 mV/Div
Y pos.(Div): 0
AC 0 DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC 0 DC -
Trigger
Edge: A B Ext
Level: 0 V
Single Normal Auto None

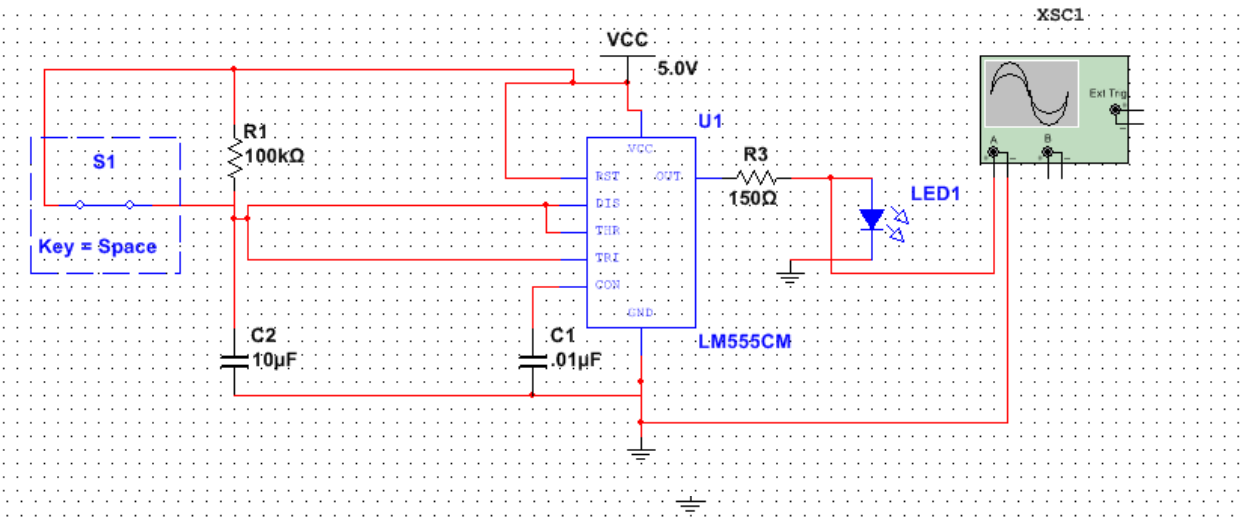

Oscilloscope-XSC1
T1
T2
T2-T1
Time
22.773 us
22.773 us
0.000 s
Channel_A
2.190 V
2.190 V
0.000 V
Channel_B
9.000 V
9.000 V
0.000 V
Reverse
Save
Ext. trigger
Timebase
Scale: 100 ns/Div
X pos.(Div): 0
Y/T Add B/A A/B
Channel A
Scale: 10 V/Div
Y pos.(Div): 0
AC 0 DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC 0 DC -
Trigger
Edge: A B Ext
Level: 0 V
Single Normal Auto None

Design of Astable Multivibrator Circuit using 555 Timer:
AIM: To construct and study the operation of a monostable multivibrator using 555 IC timer.
APPARATUS:

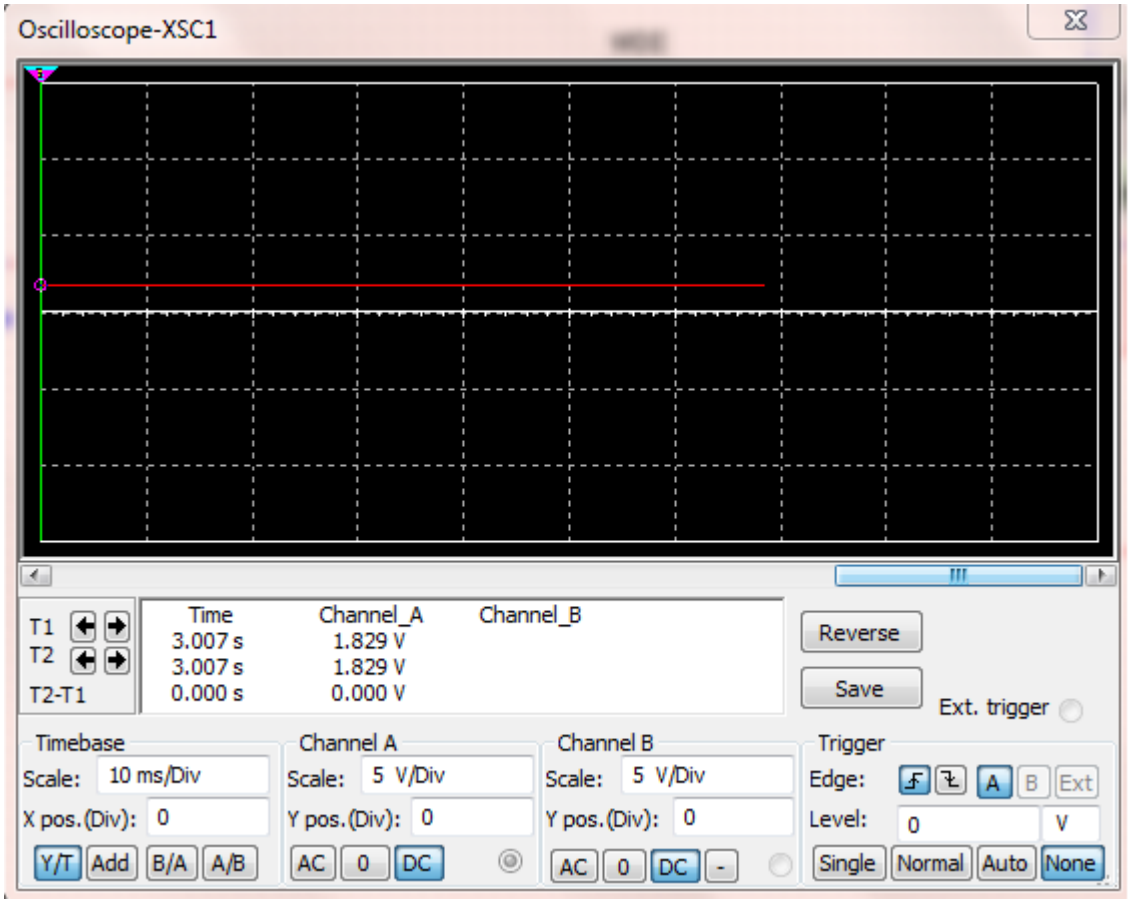
S.NO.	Name of the Equipment	Values	Quantity
1	555 IC Timer		1
2	Resistor	10 KΩ	1
3	Capacitors	10nF, 0.1μF, 0.01μF	1
4	Function Generator	1MHz	1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

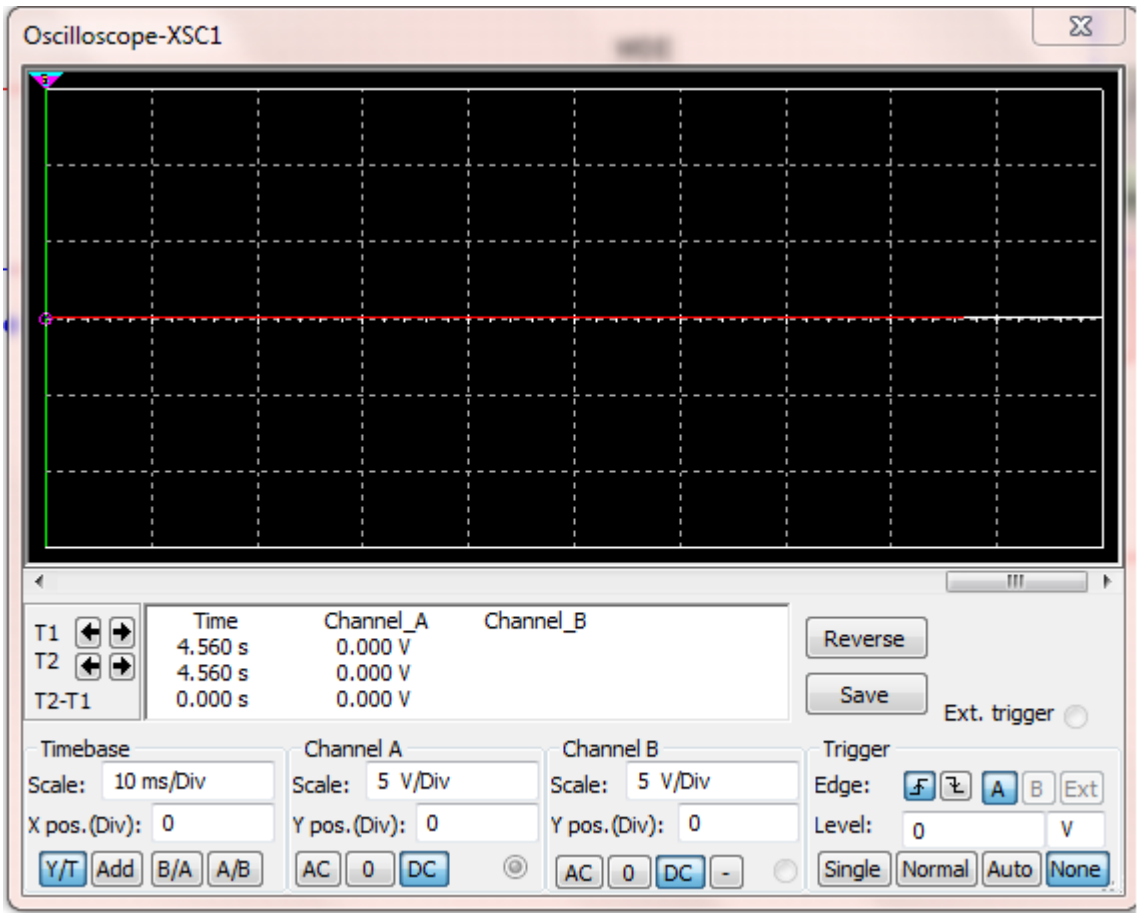
THEORY:
In the 555 Oscillator above, pin 2 and pin 6 are connected together allowing the circuit to retrigger itself on each and every cycle allowing it to operate as a free running oscillator. During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the discharge terminal, pin 7. Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the 0.693(R1+R2)C combination and discharges itself down to 1/3Vcc (the lower comparator limit) determined by the 0.693(R2.C) combination. This results in an output waveform whose voltage level is approximately equal to Vcc - 1.5V and whose output "ON" and "OFF" time periods are determined by the capacitor and resistors combinations. The individual times required completing one charge and discharge cycle of the output is therefore given as:

$$t1 = 0.693\ (R1+R2)C,\ t2 = 0.693\ R2C,\ T = t1 + t2$$



Result & Discussion: The waveform was traced and compared with the designed theoretical one.




Oscilloscope-XSC1
T1
T2
T2-T1
Time
Channel_A
Channel_B
4.560 s
0.000 V
4.560 s
0.000 V
0.000 s
0.000 V
Reverse
Save
Ext. trigger
Timebase
Scale: 10 ms/Div
X pos.(Div): 0
Y/T
Add
B/A
A/B
Channel A
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
-
Trigger
Edge:
A
B
Ext
Level: 0 V
Single
Normal
Auto
None